UNIT-1

ICs and OP-AMPs

Introduction to Integrated Circuits (ICs):

Integrated Circuit (IC):

IC is a miniature and low-costelectronic circuit consisting of active devices (Diodes, Transistors and Op-Amps), passive components (Resistors and Capacitors), joined together on a single crystal silicon chip.

Advantages of ICs over discrete circuits:

- Small size
- Low cost
- High reliability
- High performance
- High speed
- Low power consumption
- Matched devices

CLASSIFICATION OF ICS

1. Linear ICs, Digital ICs and Mixed–Signal ICs

Based on mode of operation, ICs are classified as Linear ICs, Digital ICs and Mixed-Signal ICs.

(a) Linear ICs: They are also called analog ICs. They are used to process analog signals.They are used to implement discrete circuitslike amplifiers, oscillators and filters. The basic building block of analog ICs is an operational amplifier.

(b) Digital ICs: They operate on digital signals (e.g.: Binary numbers). They are used to implement logic circuits like logic gates, counters, microprocessors, etc.

(c) Mixed–signal ICs: These are designed to process combinations of analog and digital signals. These are the most complex to design. These ICs are designed for applications like ADCs, DACs, cell phones, etc.

2. Monolithic ICs and Hybrid ICs:

Based on the method of fabrication, ICs are classified as monolithic ICs and Hybrid ICs

Monolithic ICs:

In monolithic ICs, all active and passive components are fabricated on a single silicon chip. Most of the ICs are monolithic.

Note: In Greek language, 'mono' means single and 'lithos' means stone.

Advantages of monolithic ICs:

- ✓ Low cost
- ✓ Thermal stability

Disadvantages:

- ➢ Large values of resistances and capacitances cannot be formed. But such large values are needed in some linear circuits.
- ➢ There is no method available to fabricate transformers and large values of inductors.

Hybrid ICs:

In hybrid ICs, passive components (R & C) and the interconnections between them are formed on an insulating substrate (e.g.: Glass, Ceramic). Active components and monolithic ICs are then connected to form a complete circuit.

Based on the fabrication process, hybrid ICs are further classified as **Thin–film ICs** (thickness is 50 A^o to 2500 A^o) and **Thick–film ICs**(Thickness is 125000 A^0 to 625000 A^o)

IC Chip size and Circuit Complexity

IC Chip size: At present, smallest dimensions of ICs are in the order of 10 nanometers.

Example: 'Intel' is mass–producing transistors of 14 nanometers size.

IC Chip Complexity: Electronic device technology used vacuum tubes until 1950s. Transistor was invented in 1947. Then, semiconductor technology became popular. At the beginning of 1960s, the concept of ICs was introduced. Since then, the size and complexity of ICs have increased rapidly.

Level of Integration	Number of Gates per Chip	Number of Transistors per chip	Time Period	Applications
Small Scale Integration (SSI)	3 to 30	10 to 100	1960–1965	Used to make Logic gates and Flipflops
Medium Scale Integration (MSI)	30 to 300	100 to 1000	1965–1970	Used to make Counters, Multiplexers, Adders. etc.
Large Scale	300 to	1000 to	1970–	Used to make

Integration (LSI)	3000	20,000	1980	RAM, ROM, and 8–bit Microprocessors.
Very LargeScale Integration (VLSI)	>3000	20,000 to 10^6	1980–1990	16– and 32–bit Microprocessors.
Ultra LargeScale Integration (ULSI)	———	10^6 to 10^7	1990 – 2000	64–bit Microprocessors, Virtual Reality Machines, Smart Sensors.
Giant Scale Integration (GSI)	———	> 10^7	———	———

BASIC INFORMATION OF OP-AMP

Definition: An Operational Amplifier (opamp) is a direct coupled high–gain amplifier available as an IC. It is used to amplify dc as well as ac signals.

Originally it was designed to perform mathematical operations such as addition, subtractions, multiplication and integration. Hence it was named 'Operational Amplifier'.

Opamp CircuitSymbol:

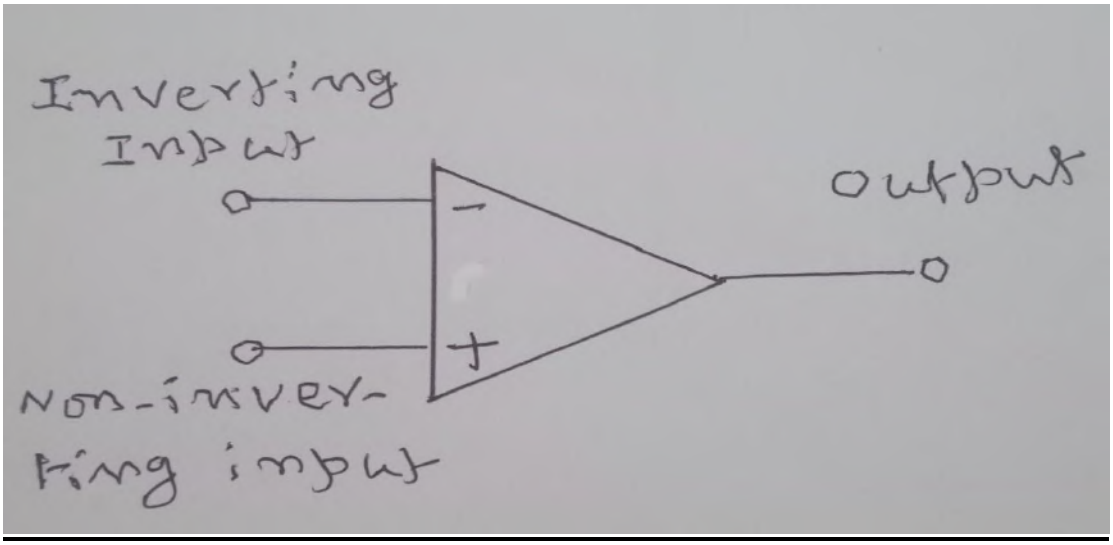


Fig.1: Opamp circuit Symbol

Types of Packages:

There are 3 basic types ofIC packages for opamps. They are:

1. Flat Pack

2. Metal Can Pack (also called ‘Transistor Pack’ or ‘TO Pack’)

3. Dual–in–line Pack

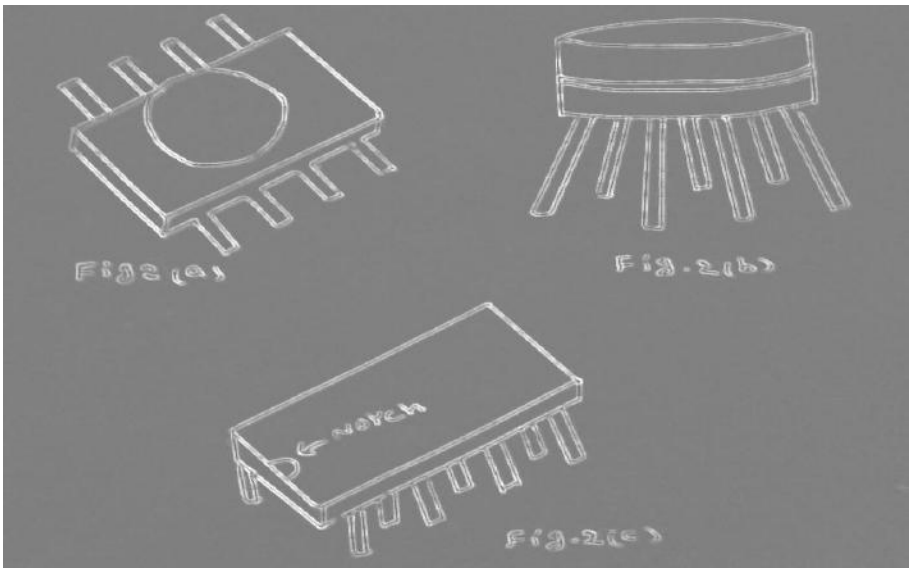


Fig. 2: Types of IC packages

1. Flat Pack: Chip is enclosed in a rectangular ceramic case. Leads extend from sides as shown in Fig. 2 (a). It comes with 8, 10, 14 or 16 leads. It is more reliable and lighter. But it has high power consumption and power dissipation

2. Metal Can Pack:

Chip is mounted in a metal or plastic case.Pins are arranged radially as shown in Fig. 2 (b). It is available with 3, 5, 8, 10 or 12 pins. It is best suited for power amplifiers and audio amplifiers. It has external heat sink to dissipate heat.

3. Dual–in–line Package (DIP):

Chip is mounted inside a plastic or ceramic case. Pins are arranged perpendicular to chip in 2 lines. It is available with 8, 12, 14, 16, 20 or 40 pins. A notch is provided to identify the pin numbers. It is suitable for mounting on PCBs. Most of the ICs come in DIP packages.

<u>Power Supply Voltages for ICs:</u>

1. Linear ICs

Most of them require both +ve and –ve supply for the circuit operation. Usually they are equal in magnitude (e.g.: +15 V and –15 V). Common point of two power supplies must be grounded. Otherwise, IC gets damaged.

A few linear ICs (earlier OP–AMPs) use unequal supply voltages. (e.g.: 720 OP–AMP). Some ICs operate with a single positive supply (e.g.: 324 OP-AMP).

2. Digital ICs:

Except ECL (Emitter Coupled Logic) family ICs, all digital ICs require only = +ve supply.

Note: some dual supply voltage opamps can also be operated from a single supply voltage by using special extra circuitry.

Labelling of power supply voltages:

It may vary from manufacturer to manufacturer.

Example:

Manufacturer	Labelling
Fairchild	V^+ and V^-
Motorola	$+V_{CC}$ and $-V_{EE}$

Equivalent Circuit of OP-AMP:

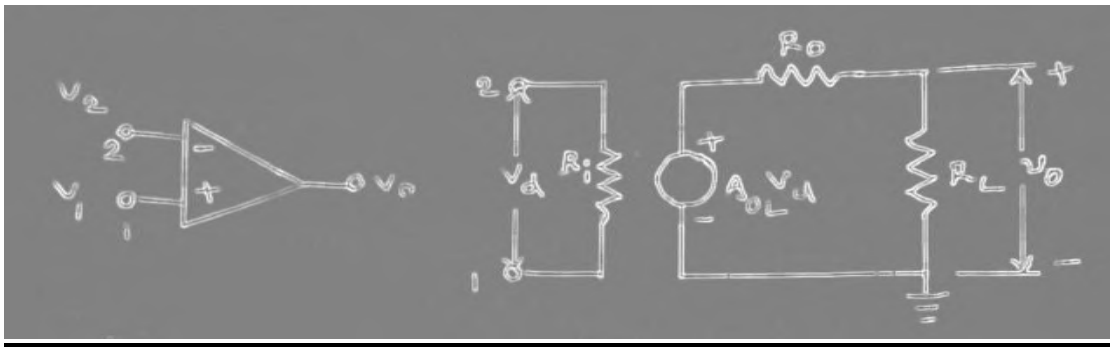


Fig. 3 (a) Fig.3 (b)

Fig. 3 (a) shows the opamp symbol. It has 2 input and 1 output terminals. Its – ve terminal '2'(in fig. 3 (a)) is called 'inverting terminal'. Its + ve terminal '1' is called 'non-inverting terminal'.

If V_1 and V_2 are the voltages measured at terminals '1' and '2' respectively w.r.t. ground, then

$(V_1 – V_2)$ is called differential-input voltage. It is denoted by 'v_d'

$(V_1 + V_2) / 2$ is called common-mode input voltage. It is denoted by 'v_c'

Equivalent Circuit of opamp:

Fig. 3 (b) presents the equivalent or internal circuit of opamp. It is the Thevenin's equivalent circuit of Fig. 3 (a). Here $A_{OL}v_d$ is 'Thevenin's equivalent voltage source' and R_o is 'Thevenin's equivalent voltage resistance' or 'output resistance'. R_i is the input resistance and R_L is the external load resistance.

Opamp has 2 supply terminals V^+ (or $+V_{CC}$) and V^- (or $-V_{EE}$). Magnitude of V^+ = Magnitude of V^-. Typical supply voltages for opamp range from ± 9 V to ± 22 V. For 741 opamp, supply voltage is ± 15 V.

The output voltage V_o is normally measured across a load resistor R_L.

V_o is given by $\mathbf{V_o = A_O v_d = A_{OL}\,(V_1 - V_2)}$

where A_{OL} is called open loop voltage gain of opamp. It is the gain when there is no feedback between input and output.

If output is fedback to input, the gain is called closed loop voltage gain. It is denoted by A_{CL}.

Note that V_o will never exceed supply voltages.

The utility (usage) of opamp is greatly increased by providing negative feedback. Then output is not driven into saturation and circuit behaves in a linear manner.

IDEAL OPERATIONAL AMPLIFIER

Ideal Opamp Characteristics:

1. Open loop voltage gain $A_{OL} = \infty$
2. Input Resistance $R_i = \infty$
3. Output Resistance Ro = 0
4. Bandwidth = ∞
5. Common Mode Rejection Ratio (CMRR) = ∞
6. Slew Rate= ∞
7. Zero Offset (i.e., if inputs V_1 and V_2 are equal, output Vo = 0)
8. Characteristics do not drift with temperature

Virtual Ground:

An ideal opamp has infinite input resistance (R_i) and infinite voltage gain (A_{OL}).

Since Ri = ∞,

No current flows through any input terminal of opamp..… (1)

Since $A_{OL} = \infty$,

$$A_{OL} = \frac{vo}{vd} = \infty$$

i.e., $$\frac{v_o}{v1 - v2} = \infty$$

i.e., $v_1 - v_2 = 0$ or $v_1 = v_2$

i.e., Both inputs are at same potential orthere exists a short circuit at the input of the opamp …. (2)

From points (1) and (2), we can say that there exists a virtual ground at the input of opamp.

It is illustrated in Fig. 5.

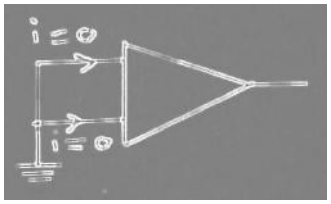


Fig.5: Virtual Ground

Operational Amplifier Internal Circuit

(Or Block Diagram of Commercial Opamp)

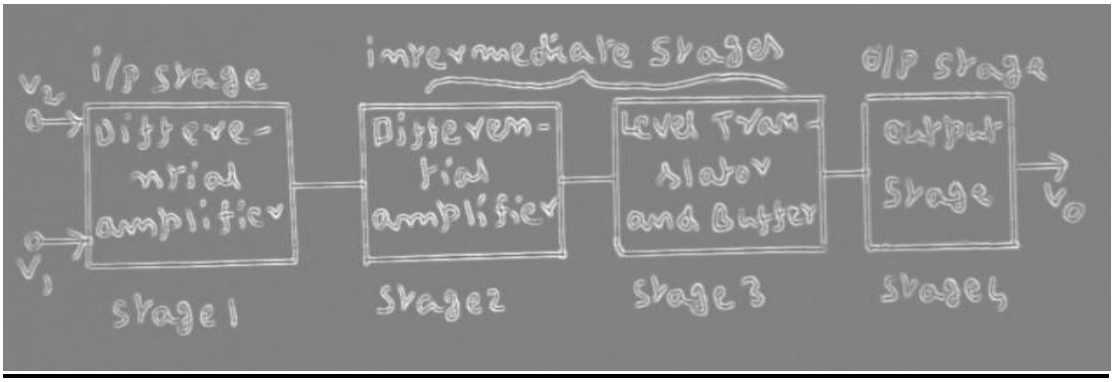


Fig. 6: Opamp Internal Circuit

Fig.6 shows the internal circuit of an opamp.

Stage1 and Stage2:

They form a cascaded differential amplifier. They provide high gain to differential signals and cancel common-mode signals.

Stage3:

It is an emitter follower supplied with constant current source. It acts as a level translator as well as a buffer.

(i) Level translator:

Because of direct coupling between stages, a dc level rises from stage to stage. It shifts the operating point of next stages. This limits the o/p voltage swing and may even distort the o/p signal.

Level translator shifts the dc level so that operating point remains the same. So, there is no distortion. It also sees that quiescent o/p voltage is zero for zero i/p signal.

(ii) Buffer:

It provides high input impedance and low output impedance. Thus, it isolates high gain stages from the o/p stage.

Stage4:

It is o/p stage. It supplies the required load current and low output impedance. A simple o/p stage is an emitter follower circuit with complementary symmetry transistors. It consists of one NPN and one PNP transistor. Their emitters are coupled as shown in Fig. 7.

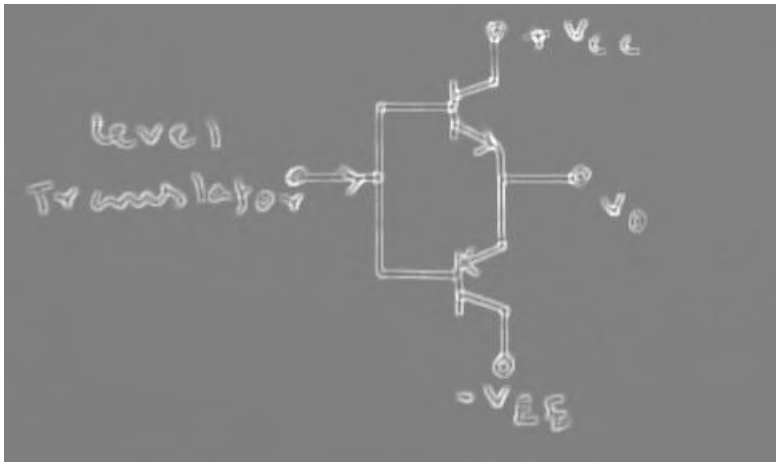


Fig. 7

DC AND AC CHARACTERISTICS OF OPAMPS

(A) DC Characteristics:

1. Input Bias Current(I_B):

It is the average of the currents that flow into the inverting (–ve) and non-inverting (+ve) terminals of opamp.

Let I_{B_1} = Current throughthe non-inverting terminal

I_{B_2} = Current throughthe non-inverting terminal

Then input bias current $I_B = \frac{I_{B1} + I_{B2}}{2}$

Its units are 'nA'. Ideally it is zero. For 741 opamp (at 25^0 C), its typical value is I_B = 80 nA

2. Input Offset Current (I_{io} or I_{os}):

It is the difference of currents entering the inverting and non-inverting terminals of opamp. It is given by

$$|I_{io}| = I_{B_1} - I_{B_2}$$

It is expressed in 'nA', Ideally it is zero. For 741 opamp (at 25^0 C) its typical value = 20 nA

3.Input Offset Voltage (V_{io} or V_{is}):

It is the voltage that must be applied between the two input terminals of opamp to balance it (i.e., to make output voltage zero). It is expressed in 'mV', Ideally it is zero. For 741 opamp (at 25^0 C) its typical value = 20 mV.

4. Maximum (orTotal) Output Offset Voltage (V_{OT}):

It is the output voltage of opamp when its two input terminals are grounded. Its value depends on whether compensating technique is used or not.

If no compensating technique is used, it is given by

V_{OT} = o/p voltage due to i/p offset voltage + o/p voltage due to i/p bias current

i.e., $V_{OT} = (1 + \frac{Rf}{R_1}) V_{io} + R_f I_B$

If a compensated resistance R_{COMP} is connected to compensate for input bias current, then

$$V_{OT} = (1 + \frac{Rf}{R_1}) V_{io} + R_f I_{io}$$

where V_{io} and I_{io} are input offset voltage and currents respectively.

IdeallyV_{OT} = 0

5. Thermal Drifts:

(i) Input Offset Current Drift:

It is the ratio of change in input offset current to the change in temperature. It is given by

$$\Delta I_{io} / \Delta T$$

It is expressed in nA/^{0}C.

(ii) Input Offset Voltage Drift:

It is the ratio of change in input offset voltage to the change in temperature. It is given by

$$\Delta V_{io} / \Delta T$$

It is expressed in mV/^{0}C.

(B) AC Characteristics

1. Frequency Response:

When frequency increases, gain of opamp reduces and phase angle between the input and output increases. This is due to the presence of integrated capacitors and stray capacitances.

Case (i): Single Corner Frequency

Let all the capacitive effects can be represented by a single capacitor 'C'. i.e., let there be a single corner frequency. Let it be 'f_1'.

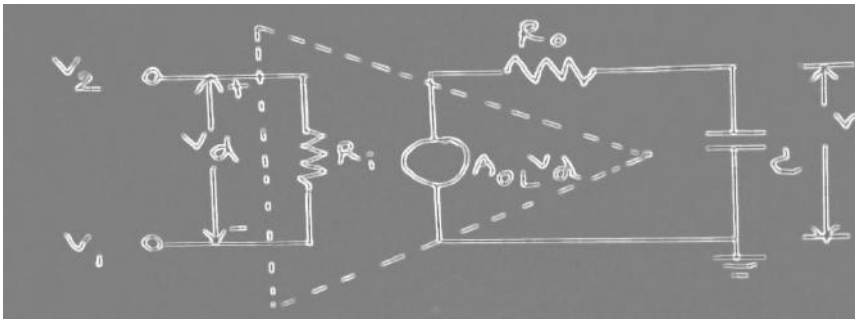


Fig.8

Fig.8 represents high frequency model of an opamp with single corner frequency. From figure, we get

$$v_o = \frac{-jX_C}{R_0 - jX_C}.\ A_{OL} v_d$$

where A_{OL} is open loop gain of opamp.

$$= \frac{-j^2 X_C}{jR_0 - j^2 X_C}.\ A_{OL} v_d \text{ (by multiplying numerator and denominator by j)}$$

$$= \frac{X_C}{jR_0 + X_C}.\ A_{OL} v_d \text{ (Since } j^2 = -1)$$

$$= \frac{1/\omega C}{jR_0 + 1/\omega C}.\ A_{OL} v_d \qquad (\text{Since } X_C = 1/\omega C)$$

Thus $v_o = \frac{A_{OL} v_d}{1 + j\omega R_0 C}$

Midband gain A = v_0 / v_d

$$= \frac{A_{OL}}{1 + j\omega R_0 C}$$

Thus A = $\frac{A_{OL}}{1+j\omega R_0 C}$

= $\frac{A_{OL}}{1+j2\pi f R_0 C}$ (because $\omega = 2\pi f$)

= $\frac{A_{OL}}{1+\frac{f}{\left(\frac{1}{2\pi R_0 C}\right)}}$

= $\frac{AOL}{1+\frac{f}{f_1}}$ …….. (1)

∴ Magnitude of A = $|A| = \frac{AOL}{\sqrt{1+\left(\frac{f}{f1}\right)^2}}$……. (2)

Phase angle $\phi = \mathbf{Tan^{-1}(f/f_1)}$ ……. (3)

Another expression for A_0:

Eq. (1) can be written as

A = $A_{OL}/(1 + j2\pi f/2\pi f_1)$

= $A_{OL}/(1 + j\omega/\omega_1)$ (Since $2\pi f = \omega$)

= $A_{OL}/(1 + s/\omega_1)$ (because jw = s)

= $\frac{A_{OL}}{s+\omega_1}$ …… (4)

From eqs. (2) and (3), we can draw the magnitude characteristics and phase characteristics

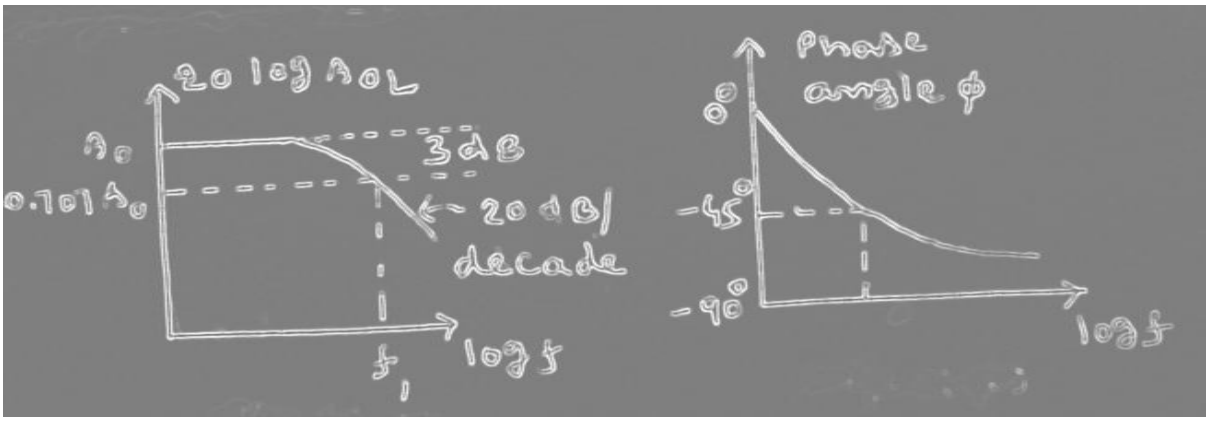


Fig.9 (a) Fig.9 (b)

(i) Magnitude Characteristics (for single corner frequency):

Fig. 9(a) represents magnitude characteristics. Frequency (in Hz) is taken on X-axis in log scale. Gain (in dB) is taken on Y-axis in linear scale.

Corner frequency 'f_1' is the frequency at which gain falls by 3 dB below its maximum value. It is also called '3 dB' frequency or 'break frequency'.

Up to f_1, gain is constant. Later it rolls off(falls) at a rate of –20dB/decade (or –6dB per octave).

Decade means 10 times increase in frequency (e.g.: Increase from 1 KHz to 10 KHz). Octave means 2 times increase in frequency (e.g.: increase from 2 KHz to 4 KHz)

(ii) Phase Characteristics:

Fig. 9 (b) shows the phase characteristics of opamp. Here X-axis represents frequency (in Hz) in log scale. Y-axis represents phases shift (in degrees) in linear scale.

Phase angle ϕ is 0^0 at 0 Hz, -45^0 at corner frequency f_1 and -90^0 at infinite frequency.

Note that zero frequency does not exist on log scale. So, for practical purposes, zero frequency is taken one decade below corner frequency. Infinite frequency means one decade above corner frequency.

Case (ii):Multiple Corner Frequencies

Since opamp has many stages, there may be different RC pole pairs. So, there will be multiple corner frequencies. Let there be three corner frequencies f_1, $f_2$and f_3. Then we can show that

$$A = \frac{A0}{\{1+j(f/f_1)\}\{1+j(f/f_2)\}\{1+j(f/f_3)\}}$$

where $0 < f_1 < f_2 < f_3$

We can also write the above equation as

$$A = \frac{A_{OL}\,\omega_1\omega_2\omega_3}{(s+\omega_1)(s+\omega_2)(s+\omega_3)}$$

Where A is overall transfer function.

For each corner frequency, phase angle increases by 90^0. When phase angle becomes 360^0, Barkhausen criterion is satisfied and oscillations are set. To prevent oscillations, we use a technique called 'frequency compensation'

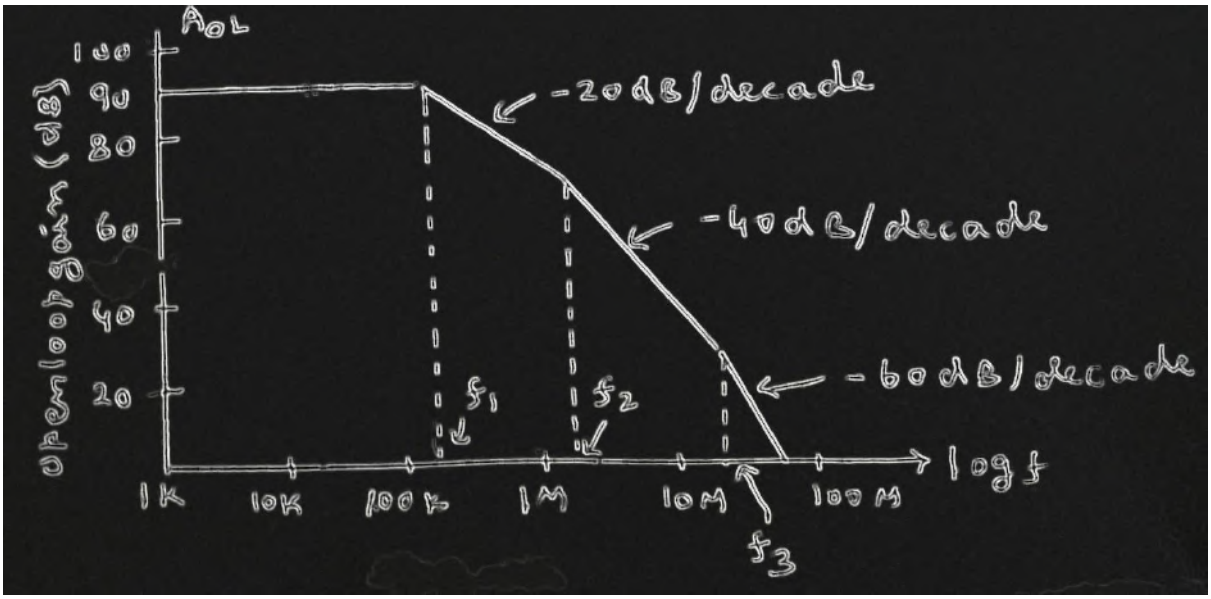


Fig.10

Fig. 10represents straight line approximation of magnitude characteristics of a typical opamp.

Here there are 3 corner frequencies. f_1 = 200 KHZ, f_2 = 2 MHz, f_3 = 20 MHz.

Up to f_1, gain is constant at 90dB. From f_1 to f_2, gain falls at a rate of –20dB/decade. From f_2 to f_3, gain falls at a rate of –40dB/decade. After f_3, gain falls at a rate of –60dB/decade.

2. Slew Rate:

Slew Rate is defined as the maximum rate of change of output voltage of an opamp. It is denoted by $\frac{dVo}{dt}$ and expressed in Volts/µSec.

For an ideal opamp, slew rate is ∞. i.e., output voltage changes simultaneously with input voltage. Practically, a capacitor is connected within or outside the opamp to prevent oscillations. Since voltage across capacitor cannot change instantaneously, $\frac{dVo}{dt}$cannot be infinite. For 741 opamp, it is 0.5 V/ µSec.

Important features of slew rate:

- It increases with increase in bandwidth.
- It increases with increase in closed loop gain.
- It increases with increase in dc supply voltage.
- It decreases with increase in temperature.
- It affects the opamp performance at high frequencies.

Slew rate is specified in data sheet at unity gain and no load. So, it is measured for a voltage follower.

3. Bandwidth:

It is the range of frequencies over which the operation of opamp is satisfactory.

For a single corner frequency f_1, gain of opamp is constant up to f_1. Therefore, Bandwidth = f_1.

4. Unity gainbandwidth:

It is defined as the bandwidth of an opamp when the voltage gain is '1'. Ideally it is infinity. Practically, it is of the order of a few MHz.

It is also called '**gainbandwidth product (GBW)'** or '**Small signal band-width'** or '**Unity gain crossover frequency'.**

5. Transient Response:

It is the immediate response of the opamp. 'Rise Time' and 'Overshoot' are two important characteristics of transient response.

(i) Rise Time:

It is the time taken by the output of opamp to change from 10% to 90% of sits maximum value. It is expressed in μSec. Ideally it is zero. for 741 opamp, its typical value is 0.3 μSec.

(ii) Overshoot: It is the deviation of the opamp output from its steady state value. It is expressed as % of output. Ideally it is zero. For 741 opamp, its typical value is 5%.

OTHER IMPORTANT TOPICS

Common Mode Rejection Ratio (CMRR):

Common-mode Signal: It is the average of the two inputs$v_1 and\ v_2$ of opamp. It is given by

$$v_c = \frac{v_1 + v_2}{2}$$

Difference-mode signal: It is the difference of two inputs of opamp. It is given by

$$v_d = v_1 - v_2$$

CMRR: It is defined as the ratio of differential gain 'A_d' to common mode gain 'A_c'. It is denoted by 'ρ' and isgiven by

$$\rho = \left| \frac{A_d}{A_c} \right|$$

Output of an opamp is given by

$$v_o = A_c v_c + A_d v_d$$

It is expressed in decibels. Ideally it is infinity. For μA 741C, it is 90 dB. It is a 'metric' or 'figure of merit' of an opamp. The higher the CMRR, the better is the performance of opamp.

Problem1.1: Determine the o/p voltage of opampfor i/p voltages of v_1= 150 μV, v_2 = 140 μV, A_d =5000 andCMRR = 20

Solution:

Output voltage $v_o = A_c v_c + A_d v_d$ … (1)

i.e., $v_o = A_d v_d \left(1 + \frac{A_c v_c}{A_d v_d}\right)$

i.e., $v_o = A_d v_d \left(1 + \frac{1}{\rho}.\frac{v_c}{v_d}\right)$ …. (2)

v_c =Common-mode signal

$= \frac{v_1 + v_2}{2} = \frac{150\ \mu V + 140\ \mu V}{2} = 145\ \mu V$

v_d =Difference-mode signal = $v_1 - v_2$

$= 150\ \mu V - 140\ \mu V = 10\ \mu V$

Given that ρ = 20 and A_d = 5000

∴ Eq. (1) ⇒

v_o = 5000 x 10 x 10^{-6} $\left(1 + \frac{1}{20} \text{ x } \frac{145\ X\ 10^{-6}}{10\ x\ 10^{-6}}\right)$

= 53.625 mV

<u>Power Supply rejection Ratio (PSRR):</u>

It is defined as the ratio of change in input offset voltage of opamp to the change in supply voltage. It is given by

$$\text{PSRR} = \Delta V_{io} / \Delta V$$

where V is the supply voltage.

It is expressed in 'μV/V' or in 'dB'.

For μA 741 C, PSRR + 150 V/μV

The lower the value of PSRR, the better the opamp.

Note: It is also called '**Supply Voltage Rejection Ratio (SVRR)' or 'Power Supply Sensitivity (PSS)'.**

Offset Balancing Techniques:

When both inputs are grounded o/p of an opamp should be ideally zero. But, practically there exists a very small o/p voltage called output offset voltage. **It is due to the input bias current 'I_B' or input offset voltage 'V_{io}' or 'V_{os}').**

To nullify (cancel or balance) the o/p offset voltage, many opamps come with a potentiometer between pins 1 and 5 of opamp. Manufacturer provides it. The position of wiper is adjusted to nullify the o/p offset voltage.

If an opamp has no such provision, we use external balancing techniques. They are called 'Universal Balancing Techniques'.

Universal Balancing Techniques:

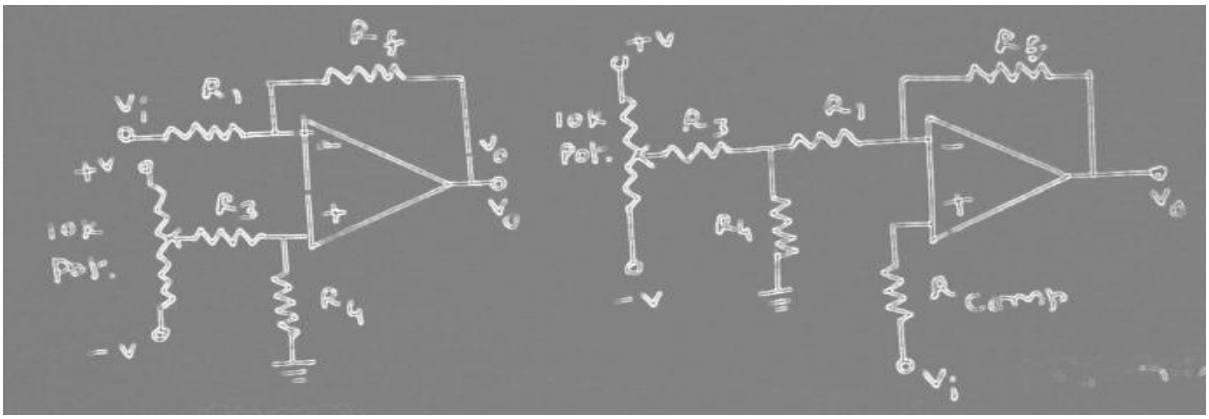


Fig. 11 (a) Forinverting Amplifier **Fig. 11 (b) Foe non-inverting Amplifier**

Fig. 11 (a) and Fig. 11 (b) show the universal balancing techniques for inverting and non-inverting amplifiers respectively

In case of non-inverting amplifier, we connect a resistor to the (+) terminal of opamp. It is shown in Fig. (b). The value of R_{comp} is given by

$R_{comp} = R1 \| Rf$

R_{comp} is connected to reduce the effects of input bias current I_B

Problem on maximum or total o/p offset voltage V_{OT}:

Problem 1.2:

(a) For the non-inverting amplifier of Fig. (b), R_1 = 1 KΩ, R_f = 10 KΩ. Calculate the maximum output offset voltage due to
V_{ios} and I_B. The opamp is LM 307 with V_{ios} = 10 mV and I_B = 300 nA, I_{os} = 50 nA.

(b) Calculate the value of R_{comp} needed to reduce the effect of I_B.

(c) Calculate the maximum output offset voltage if the above calculated $R_{comp}$is connected in the circuit.

Solution:

(a) It is the output voltage of opamp when its two input terminals are grounded. Its value depends on whether compensating technique is used or not.

If no compensating technique is used, V_{OT} is given by

V_{OT} = o/p voltage due to i/p offset voltage + o/p voltage due to i/p bias current

i.e., $V_{OT} = (1 + \frac{Rf}{R_1}) V_{io} + R_f I_B$

$= (1 + \frac{10 \times 10^3}{1 \times 10^3}) 10 \times 10^{-3} + 10 \times 10^3 \times 300 \times 10^{-9}$

$= 110 \times 10^{-3} + 3 \times 10^{-3} = 113$ mV

(b) The value of R_{comp} needed is

$R_{comp} = R1 \parallel Rf$

$= 1\ K\Omega \parallel 10\ K\Omega = 990\ \Omega$

(c) With R_{comp} in the circuit

$V_{OT} = (1 + \frac{Rf}{R_1}) V_{io} + R_f I_{io}$

$= 110 \times 10^{-3} + 10 \times 10^3 \times 50 \times 10^{-9}$

$= (110 \times 10^{-3} + 0.5 \times 10^{-3}) V$

$= 110.5$ mV

Note: From the above example, it can be seen that V_{io}contributes more to the V_{OT}compared to I_B or I_{io}

<u>Derivation for formula of Slew Rate:</u>

Slew rate is expressed in data sheets for unity gain opamp with no load.

Unity gain means Gain = 1 or output voltage = input voltage

i.e., Vo = Vi …. (1)

Let input = V_m Sin ωt … (2)

Eqs. (1) and (2) ⇒

$V_o = V_m \sin \omega t$

$\frac{dV_o}{dt} = \omega V_m \cos \omega t \quad \ldots (3)$

Slew rate = $\left| \frac{dV_o}{dt} \right|_{max}$

It occurs at $\cos \omega t = 1$

i.e., Slew rate = $\left| \frac{dV_o}{dt} \right|_{max}$ at $\cos \omega t = 1$

$= \omega V_m . 1 \ldots\ldots$ [from eq. (3)]

$= \omega V_m = 2\pi f V_m$ Volts/Sec (Since $\omega_m = 2\pi f$)

$= \frac{2\pi f V_m}{10^6}$ Volts/µSec

where f = input frequency

Thus, Slew rate = $2\pi f V_m$ Volts/Sec = $\frac{2\pi f V_m}{10^6}$ Volts/µSec

Problems on slew rate:

Problem 3.3: The o/p voltage of certain opamp circuit changes by 20 V in 4 micro seconds. What is slew rate?

Solution:

Slew rate = $\frac{dV_o}{dt} = \frac{20\ V}{4\ x\ \text{Sec}} = 5$ Volts/µSec

Problem 3.4: Assume that 741 opamp is connected as a unity gain inverting amplifier. Let the input change be 8 V. Determine the time taken for the output to change by 8 V.

Solution:

For 741 opamp Slew rate = 0.5 Volts/µSec

i.e., $\frac{dV_o}{dt} = 0.5$ Volts/µSec

Given that $dV_o = 10$ V

i.e., $\frac{10}{dt} = 0.5$ Volts/µSec

i.e., dt = $\frac{10\ V}{0.5\ V/\mu Sec}$

= $\frac{10}{0.5}$ x 10^{-6} Sec

= 20 x 10^{-6} Sec = 20 µSec

µA741 opamp and its features

- It is manufactured by Fairchild Corporation. µA is the manufacturer'sidentification code.
- It is a monolithic IC constructed using planar epitaxial process.
- It is used for many linear applications and some non-linear applications. It is internally frequency compensated.
- It has high gain, high bandwidth, low power consumption and gives better performance.
- It has short circuit protection and "offset" null capability
- It comes in 3 IC packs: 8-pin metal can, 10-pin flat pack and 8- or 10-pin DIP.
- It is available in different classes such as A, C, E, S and SC.
- Manufacture data sheet specifies two sets of electrical characteristics.

Pin Diagram of µA741 opamp:

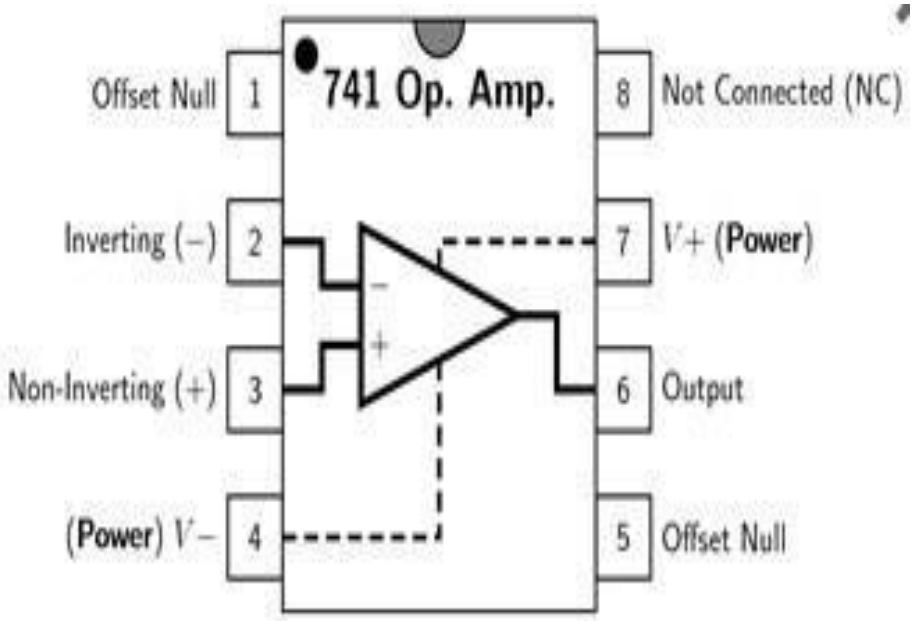


Fig. 4: Pin diagram

Classes of 741 opamps:

741 opamp is available in different classes such as A, C, E, S and SC.

(a) Military grade:

741: Military grade opamp (temperature range is -55^0 to 125^0 C)

741A: Improved version of 741

741S: Opamp with high slew rate

(b) Commercial grade:

741C: Commercial grade opamp (temperature range is -0^0 to 70^0 / 75^0 C)

741E: Improved version of 741C

741SC: Opamp with high slew rate

Military graded ICs are costly, but have superior quality. Commercial graded ICs are cheaper but have more tolerances.

***** Completed*****

QUESTION BANK (UNIT-1)

Content of Descriptive Questions

1. What is an Integrated Circuit? What are its advantages over discrete circuits? Describe the classification of ICs
2. What is an Operational Amplifier? Why it is called so? (Why it is named so?) Describe the equivalent circuit of an opamp.
3. Describe various levels of integration of ICs? What are the characteristics of an Ideal Opamp?
4. Draw and explain the internal circuit of an operational amplifier.
5. Describe the DC characteristics of an operational amplifier.
6. Describe the AC characteristics of an operational amplifier.

Note: A problem may also be given with any question.

2 Marks Questions

1. Define an IC.
2. What is an operational amplifier?
3. What are the characteristics of an Ideal Opamp?
4. Distinguish among linear ICs, digital ICs and mixed–signal ICs.
5. What are various types of IC packages?
6. Draw the equivalent circuit of an opamp.
7. Describe the concept of virtual ground of an opamp.
8. Define the corner frequency of an opamp.

9. What is Slew rate?
10. What is CMRR?
11. What is PSRR (SVRR)?
12. Define (or what is) input bias current?
13. Define (or what is) input offset current?
14. Define (or what is) input offset voltage?
15. Define (or what is) output offset voltage?
16. Define input offset current drift and input offset voltage drift.
17. What is the difference between open loop opamp and closed loop opamp?
18. Why opamp is named so?
19. Define rise time and overshoot of an opamp.
20. Draw the pin diagram of 741 opamp.

Objective Questions

1. A linear IC is also called --------- IC.
   (a) Analog (b) Digital (c) Discrete (d) None
2. Digital ICs process ----------
   (a) Voltages (b) Analog signals **(c) Digital signals** (d) Mixed input signals
3. What is the advantage of an IC over a discrete circuit?
   (a) High reliability (b) Better performance (c) High speed **(d) All of the above**
4. ULSI stands for
   (a) Urgent Linear Scale Integration **(b) Ultra Large Scale Integration**(c)Universal Large Scale Integration (d) Unknown Large Scale Integration
5. An opamp can amplify ----- signals.
   (a) AC (b) DC **(c) Both** (d) None
6. Which is the most popular IC package?
   (a) Flat Pack
   (b) Metal Can Pack
   (c) TO Pack
   (d) Dual–in–line Pack
7. The stages in an opamp are ------ coupled.
   (a) Resistor (b) Capacitor**(c) Direct** (d) Transformer
8. A buffer stage provides ------ input impedance and ------ output impedance
   (a)High, low (b) Low, low (c)High, high (d) Low, high
9. If I_{B_1} and I_{B_2} are the currents entering and inverting and non-inverting terminals of opamp, the value of input bias current is
   (a) $\boldsymbol{I_{B_1} - I_{B_2}}$ (b) $\frac{I_{B_1}+I_{B_2}}{2}$ (c) $I_{B_1} I_{B_2} +$ (d) I_{B_1}/I_{B_2}
10. If I_{B_1} and I_{B_2} are the currents entering and inverting and non-inverting terminals of opamp, the value of input offset current is

(a) $I_{B_1} - I_{B_2}$ **(b)** $\frac{\boldsymbol{I_{B_1} + I_{B_2}}}{\boldsymbol{2}}$ (c) $I_{B_1} I_{B_2} +$ (d) I_{B_1} / I_{B_2}

11. What is the order of input bias current?
    (a) mA (b) μA **(c) nA** (d) Amperes
12. One octave means
    (a) 8 times the frequency (b) 4 times the frequency (c) 10 times the frequency **(d) 2 times the frequency**
13. One decade means
    (a) 8 times the frequency (b) 2 times the frequency **(c) 10 times the frequency** (d) 4 times the frequency dsf
14. To prevent oscillations a -------- is connected within or outside the opamp
    (a) Resistor (b) Inductor **(c) Capacitor** (d) None
15. Slew rate decreases with increase in ------
    (b) A_{CL} (b) DC Supply voltage (c) Bandwidth **(d) Temperature**
16. If v_1 and v_2 are the two inputs of an opamp, the common-mode signal is
    (a) $\frac{\boldsymbol{v_1 + v_2}}{\boldsymbol{2}}$ (b) $v_1 - v_2$ (c) $v_1 + v_2$d (d) $\frac{v_1 - v_2}{2}$
17. Power Supply Rejection Ratio is given by
    (a) $\Delta V_{io} / \Delta T$ (b) $\Delta V_{io} / \Delta T$ (c) $\Delta I_{io} / \Delta V$ **(d)** $\boldsymbol{\Delta V_{io} / \Delta V}$
18. R_{comp} is connected to reduce the effects of input bias current I_B
    (a) Input offset current **(b) Input bias current** (c) Input offset voltage (d) Gain of an opamp
19. μA741 opamp is available as a ------ IC
    (a)Thin-film(b) Thick-film **(c)Monolithic** (d) Not available as an IC
20. –40 dB/decade means ------
    (a) – 6 octaves per decade **(b) – 12 octaves per decade** (c) – 18 octaves per decade (d) – 24 octaves per decade

Unit-2

Linear Applications of opamps

Inverting Amplifier

Fig.1 represents an inverting amplifier. Here input signal (ac or dc) is applied to the (-) input of opamp through resistor R_1. (+) terminal is grounded. Output voltage Vo is fed back to (-) terminal through feedback resistor R_f.

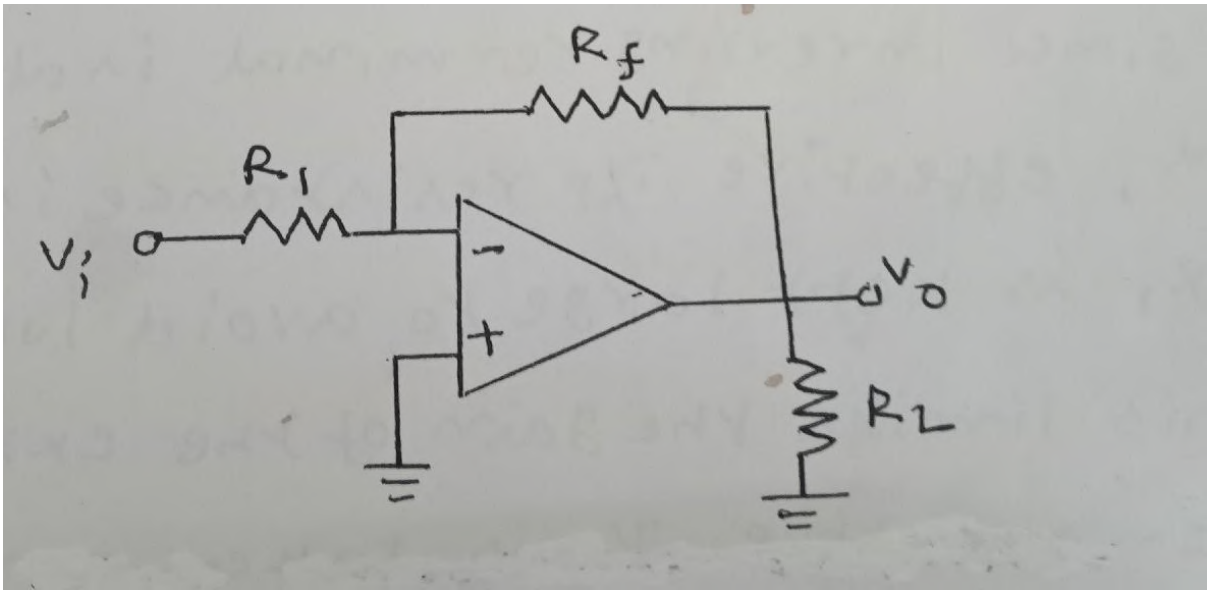


Fig.1: Inverting Amplifier

Consider nodes ‘a’ and ‘b’. Nodal equation at node ‘a’ is

$$\frac{v_a - v_i}{R_1} + \frac{v_a - v_o}{R_f} = 0 \ \ldots\ldots\ldots(1)$$

Let opamp be ideal. i.e., there exists a virtual short circuit at the input of opamp.

$$\text{i.e., } v_a = v_b = 0$$

∴Eq. (1) becomes

$$\frac{0 - v_i}{R_1} + \frac{0 - v_o}{R_f} = 0$$

$$-\frac{v_i}{R_1} - \frac{v_o}{R_f} = 0$$

i.e., closed loop gain is

$$\therefore \mathbf{A_{CL}} = \frac{\boldsymbol{v_0}}{\boldsymbol{v_i}} = -\frac{\boldsymbol{R_f}}{\boldsymbol{R_1}}$$

The $-$ ve sign indicates that v_o is 180^0 out of phase with v_i.

The gain A_{CL} can be adjusted by proper selection of R_1 and R_f.

Problem 2.1: Design an amplifier using opamp with a gain of -10.

Solution:

Since closed loop gain A_{CL} is -ve, it is an inverting amplifier.

$\therefore A_{CL} = -R_f/R_1 = -10$

Choose $R_1 = 10$ KΩ

i.e., $R_f = 10R_1 = 10 \times 10 = 100$ KΩ

Non-Inverting Amplifier

Fig. 2 (a) represents a non-inverting amplifier. Here input signal v_i (ac or dc) is applied to the non-inverting terminal. Output v_o is feedback to inverting terminal through feedback resistor R_f.

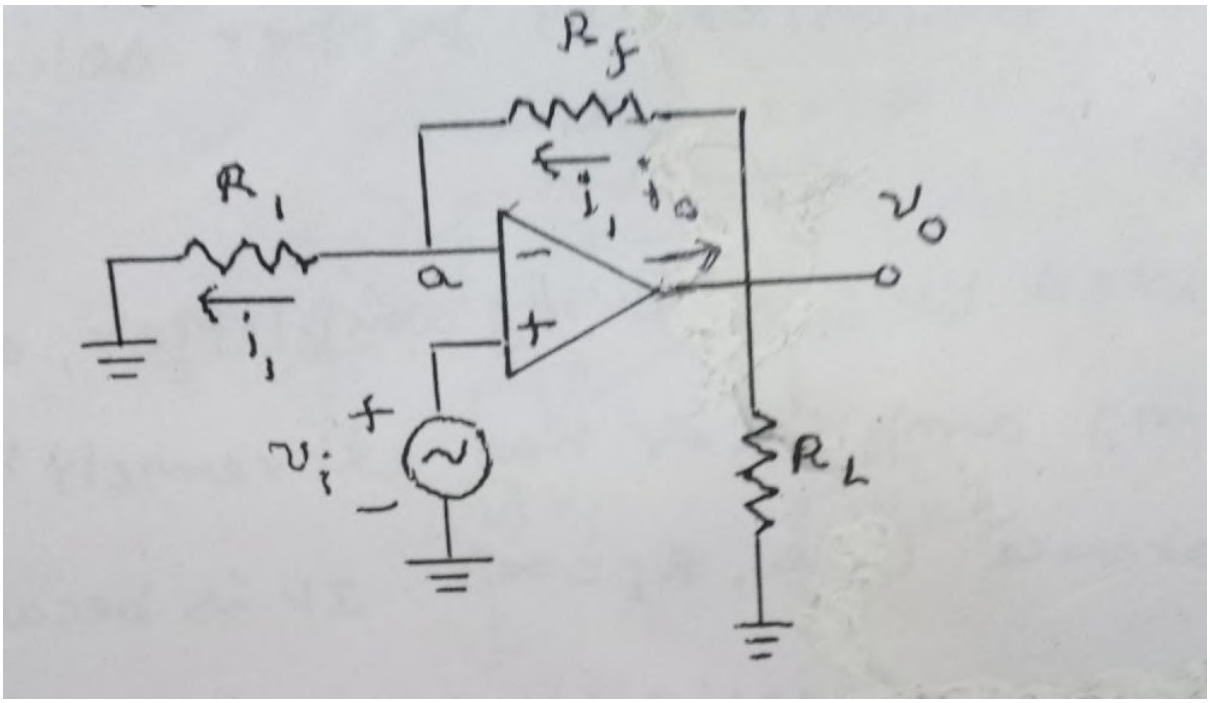


Fig. 2 (a): Non-Inverting Amplifier

Consider node 'a' as shown.

Nodal equation at node 'a' is

$$\frac{v_a - 0}{R_1} + \frac{v_a - 0}{R_f} = 0 \quad \ldots\ldots (1)$$

Let the opamp be ideal. i.e., there exists a virtual short circuit at the input of opamp.

$$\text{i.e., } v_a = v_i$$

∴ Eq. (1) becomes

$$\frac{v_i - 0}{R_1} + \frac{v_i - 0}{R_f} = 0$$

$$\text{i.e., } v_i\left(\frac{1}{R_1} + \frac{1}{R_f}\right) = \frac{v_o}{R_f}$$

$$\left(\frac{R_1 + R_f}{R_1 R_f}\right) v_i = \frac{v_o}{R_f}$$

$$\text{i.e., } \mathbf{A_{CL}} = \frac{\boldsymbol{v_o}}{\boldsymbol{v_i}} = \frac{\boldsymbol{R_1 + R_f}}{\boldsymbol{R_1}} = \mathbf{1} + \frac{\boldsymbol{R_1}}{\boldsymbol{R_f}}$$

A_{CL} can be adjusted by proper selection of R_1 and R_2

Note: Compared to inverting amplifier, a non-inverting amplifier has extremely high input resistance (i.e., Ri = ∞). It is because the opamp draws negligible current from the signal source.

Voltage Follower

Consider the non-inverting amplifier shown in Fig. 2. If $R_f = 0$ and $R_1 = \infty$, we get the circuit shown in Fig. 2 (b)

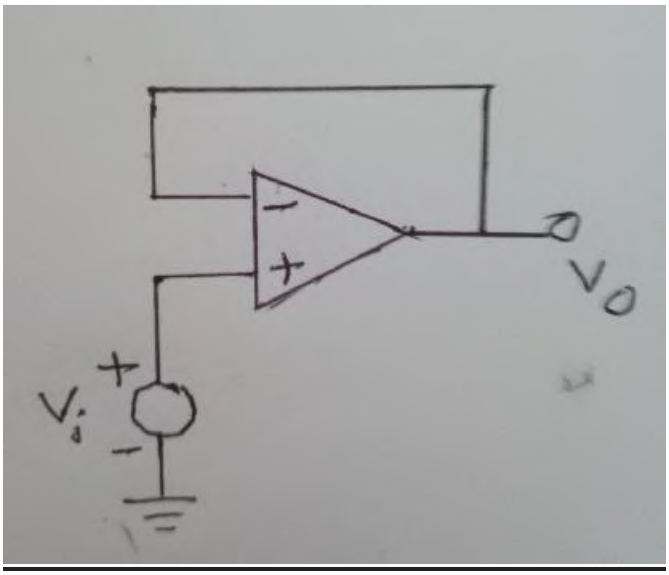


Fig. 2 (b) Voltage follower

Consider node 'a' as shown.

Since it is shorted to v_o,

$v_a = v_o$ ……. (1)

Let opamp be ideal. i.e., there exists a short circuit at its input.

i.e., $v_a = v_i$ …… (2)

Eqs. (1) and (2) $\Rightarrow$

$\mathbf{v_o = v_i}$

i.e., o/p voltage is equal to i/p voltage, both in phase and magnitude.

In other words, o/p voltage follows i/p voltage.

Hence, the circuit is called a voltage follower.

Applications of voltage follower:

Voltage follower has very high i/p impedance (order of MΩ) and low o/p impedance. Thus, it is used as a buffer for impedance matching, that is, to connect a high impedance source to low impedance load.

Problem 2.2: Design an amplifier using one opamp with a gain of + 5.

Solution:

Since gain A_{CL} is = + ve, it is a non-inverting amplifier.

$\therefore A_{CL} = 1 + \frac{R_f}{R_1} = 5$

i.e., $\frac{R_f}{R_1} = 5\text{-}1 = 4$

or $R_f = 4\ R_1$

Choose $R_1 = 10\ K\Omega$

$\therefore R_f = 4 \times 1\ K\Omega = 4\ K\Omega$

Summer or Adder

(a) Inverting summer:

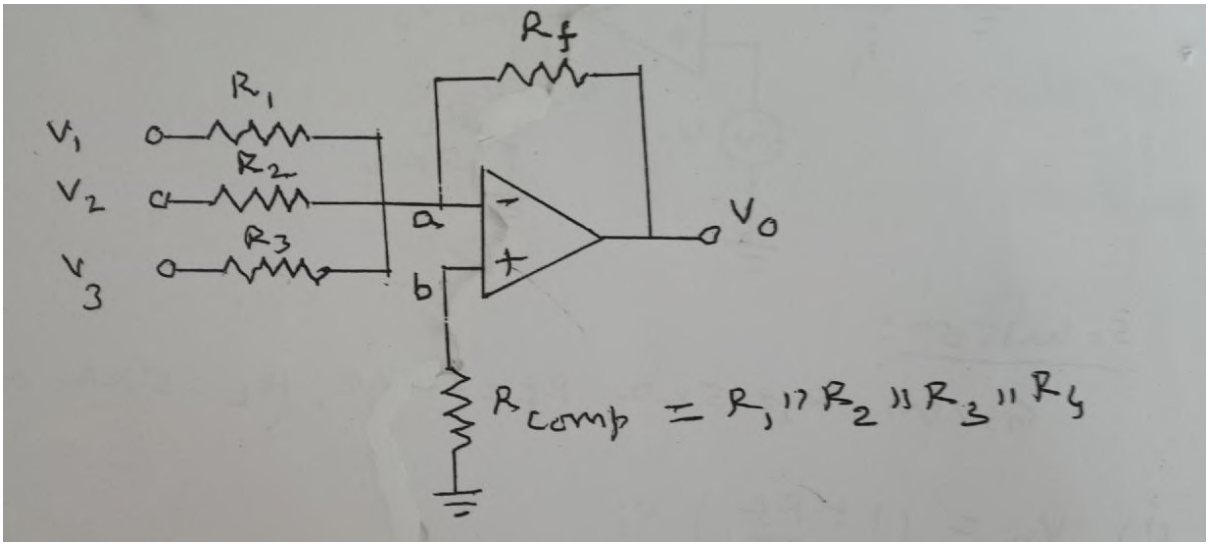


Fig.3: Inverting Summer

Fig. 3 shows an inverting summing and scaling amplifier. (Scaling factor or weight here means multiplication factor). Here V_1, V_2 and V_3 are 3 input voltages. R_1, R_2 and R_3 are input resistors. V_O is the output voltage and R_f is feedback resistor.

Consider nodes 'a' and 'b' as shown.

Nodal equation at node 'a' is

$$\frac{v_a - v_1}{R_1} + \frac{v_a - v_2}{R_2} + \frac{v_a - v_3}{R_3} + \frac{v_a - v_o}{R_f} = 0 \ldots\ldots (1)$$

Let opamp be ideal. i.e., there exists a virtual short circuit at the input of opamp.

$$\text{i.e., } v_a = v_b = 0$$

$\therefore$Eq. (1) becomes

$$-\frac{v_1}{R_1} - \frac{v_2}{R_2} - \frac{v_3}{R_3} = \frac{v_o}{R_f}$$

$$\text{i.e., } v_o = -R_f \left(\frac{v_1}{R_1} + \frac{v_2}{R_2} + \frac{v_3}{R_3} \right) \quad \ldots\ldots\ldots (2)$$

i.e., output is inverted and weighted sum of the inputs.

Special Cases:

Case (i): Let $R_1 = R_2 = R_3 = R_f = R$

∴ Eq. (2) becomes

$$v_o = -R \left(\frac{v_1}{R} + \frac{v_1}{R} + \frac{v_1}{R} \right) = -(v_1 + v_2 + v_3)$$

i.e., output is the inverted sum of inputs. So, the circuit is a **simple summer** circuit.

Case (ii): $R_1 = R_2 = R_3 = 3R_f$

∴ Eq. (2) becomes

$$v_o = -R_f \left(\frac{v_1}{3R_f} + \frac{v_2}{3R_f} + \frac{v_3}{3R_f} \right)$$

i.e., $v_o = -(v_1 + v_2 + v_3)/3$

i.e., output is the inverted average of the inputs. so, this circuit is called an **averaging amplifier.**

(b) Non-Inverting Summer

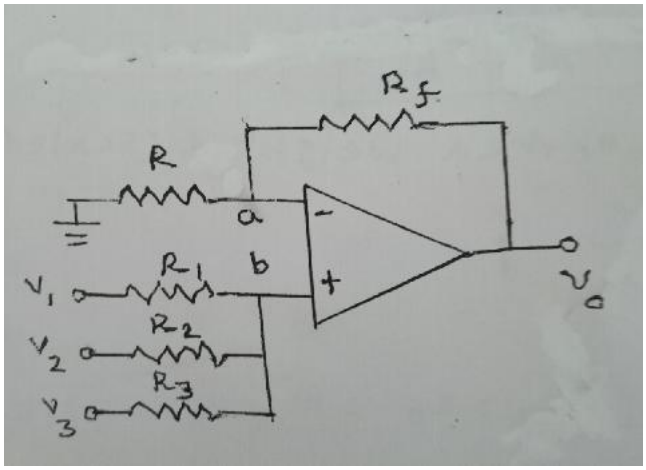


Fig.4: Non-Inverting Summer

Fig. 4 shows a non-inverting summing and scaling amplifier. Here V_1, V_2 and V_3 are 3 input voltages. R_1, R_2 and R_3 are input resistors. V_O is the output voltage and R_f is feedback resistor.

Consider nodes 'a' and 'b' as shown.

Nodal equation at node 'a' is

$$\frac{v_b - v_1}{R_1} + \frac{v_b - v_2}{R_2} + \frac{v_b - v_3}{R_3} = 0 \quad \ldots\ldots (1)$$

Let opamp be ideal. i.e., there exists a virtual short circuit at the input of opamp.

$$\text{i.e., } v_b = v_a = 0$$

∴Eq. (1) becomes

$$\frac{v_a - v_1}{R_1} + \frac{v_a - v_2}{R_2} + \frac{v_a - v_3}{R_3} = 0$$

$$\text{i.e., } v_a \left(\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3}\right) = \frac{v_1}{R_1} + \frac{v_2}{R_2} + \frac{v_3}{R_3}$$

$$\text{i.e., } v_a = \left(\frac{v_1}{R_1} + \frac{v_2}{R_2} + \frac{v_3}{R_3}\right) \Big/ \left(\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3}\right) \ldots\ldots (2)$$

Since it is a non-inverting amplifier

$$A_{CL} = \frac{v_o}{v_a} = 1 + \frac{R_f}{R}$$

$$\text{i.e., } v_o = \left(1 + \frac{R_f}{R}\right) \left(\frac{v_1}{R_1} + \frac{v_2}{R_2} + \frac{v_3}{R_3}\right) \Big/ \left(\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3}\right)$$

$$\ldots\ldots (3)$$

Eq. (3) is of the form

$$v_o = K \left(\frac{v_1}{R_1} + \frac{v_2}{R_2} + \frac{v_3}{R_3}\right)$$

Where $K = \left(1 + \frac{R_f}{R}\right) / \left(\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3}\right)$

i.e., output is non-inverted weighted sum of input.

Special Case:

Let $R_1 = R_2 = R_3 = R = \frac{R_f}{2}$ (i.e., $R_f = 2R$)

Then eq. (3) becomes

$$v_o = (1 + \frac{2R}{R}) \left(\frac{v_1}{R} + \frac{v_2}{R} + \frac{v_3}{R}\right) \Big/ \left(\frac{1}{R} + \frac{1}{R} + \frac{1}{R}\right)$$

$= 3\frac{1}{R}(v_1 + v_2 + v_3) / \frac{3}{R}$

$= v_1 + v_2 + v_3$

i.e., Output is the non-inverted sum of inputs. So, the circuit is called **a non-inverting summer circuit.**

Subtractor (Or Difference Amplifier)

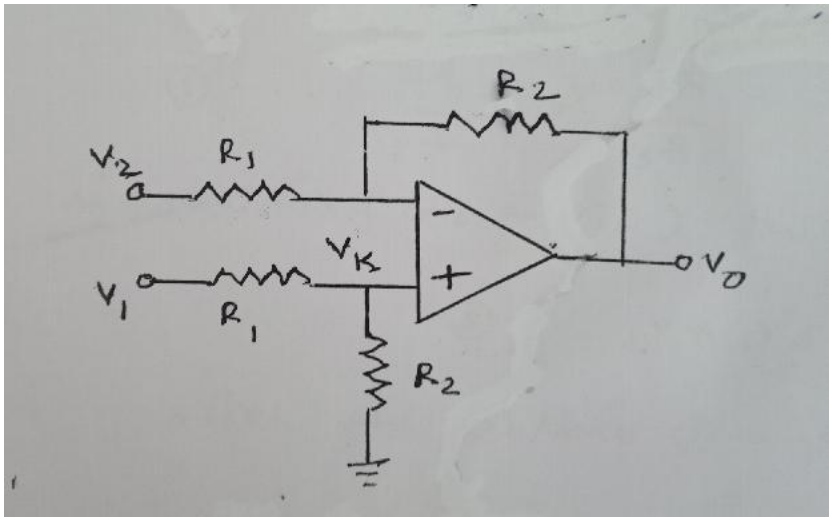


Fig.5: Subtractor

Fig. 5 shows an opamp subtractor circuit. Let v_k be the voltage at the (+) terminal of opamp. then

$$\text{Then } v_k = v_1 \frac{R_2}{R_1 + R_2} \quad \ldots\ldots\ (1)$$

By applying super position theorem, we get

$$v_o = v_k (1 + \frac{R_2}{R_1}) + v_2 \left(\frac{-R_2}{R_1}\right)$$

$$= v_k \left(\frac{R_1 + R_2}{R_1}\right) - v_2 R_2 / R_1 \ldots\ldots\ldots\ldots\ (2)$$

Putting the value of v_k from eq. (1) in to eq. (2), we get

$$v_o = v_1 \frac{R_2}{\cancel{R_1 + R_2}} \frac{\cancel{R1+R2}}{R_1} - v_2 \frac{R_2}{R_1}$$

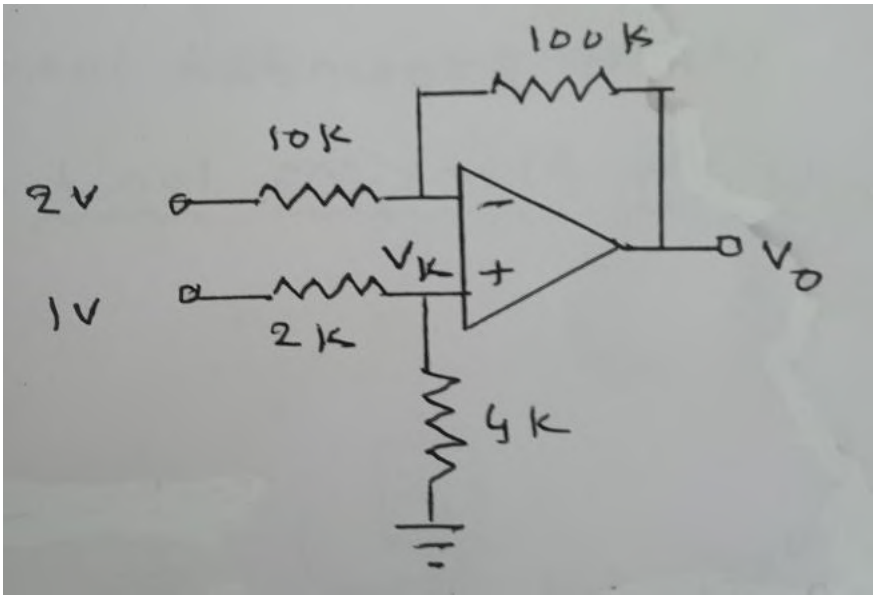
$$= \frac{R_2}{R_1} (v_1 - v_{2)}$$

If $R_1 = R_2$, then

$$\mathbf{v_o = v_1 - v_2}$$

Thus, the circuit acts as a difference amplifier (or subtractor).

Problem 2.3: find the output of the following circuit



Let vk be the voltage at the non-inverting terminal of the given circuit.

$\therefore_{vk} = 1 \times \frac{4}{4+2} = 2/3$ V

Applying superposition theorem, we get

$v_o = v_k (1 + \frac{100\ K}{10\ K}) + 2 (\frac{-100\ K}{10\ K})$

$= v_k (1 + 10) - 2 \times 10$

$= 11\ vk - 20$

$= 11 \times \frac{2}{3} - 20$

$= 7.33 - 20$ m$= -12.67$ V

Voltage to Current (V to I) Converter

(Transconductance Amplifier)

In many applications we need to convert voltage signal to appropriate current signal. This can be done using a Voltage to Current (V to I) Converter. Based on the type of load, V to I converters are of two types.

(i) V to I converter with floating load

(ii) V to I converter with grounded load

(i) V to I converter with floating load:

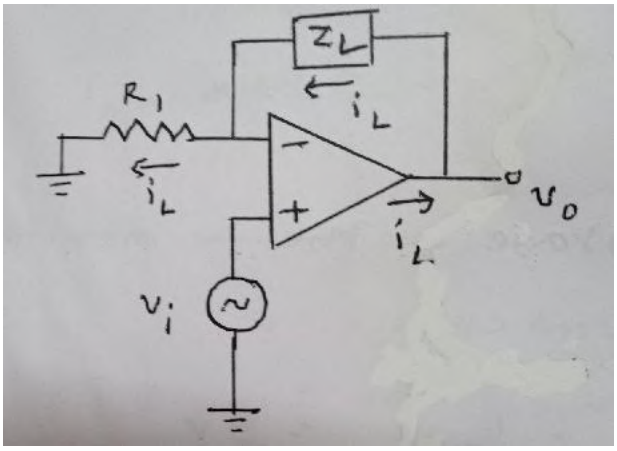


Fig.6 (a): V to I converter with floating load

Fig. 6 (a) represents a V to I converter with floating load Z_L. i.e., no end of Z_L is grounded. Assuming ideal opamp, from Fig. 6, we write

$$\frac{v_i - 0}{R_1} = i_L$$

Where v_i is input voltage, R_1 is input resistor and i_L is load current.

$$\text{i.e., } \mathbf{i_L = \frac{v_i}{R_1}}$$

i.e., i/p voltage v_i is converted to an o/p current $\frac{v_i}{R_1}$

(ii) V to I converter with grounded load

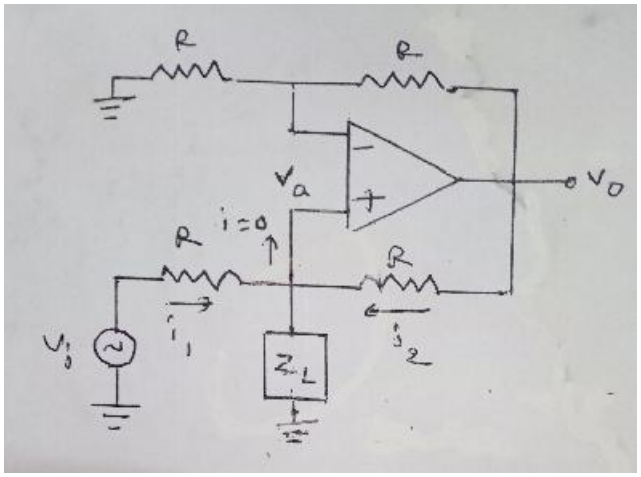


Fig. 6 (b)V to I converter with grounded load

Fig. 6 (b)represents an V to I converter with grounded load Z_L. i.e., one end of Z_L is grounded.

Let v_a be the voltage at (+) terminal of opamp.

From Fig.6 (b), we get**current downwards through Z_L** is$i_L = i_1 + i_2$ ……. (1)

But $i_1 = \frac{v_i - v_a}{R}$ ……. (2) and $i_2 = \frac{v_o - v_a}{R}$ …… (3)

But $i_L = \frac{v_i - v_a}{R} + \frac{v_o - v_a}{R} = \frac{v_i + v_o - 2v_a}{R}$ ……. (4)

But gain of opamp = 1 + R/R = 2 = $\frac{v_0}{v_a}$

i.e., $v_o = 2\,v_a$…... (5)

Eqs. (4) and (5) $\Rightarrow i_L = \frac{v_i + 2v_a - 2v_a}{R} = \frac{v_i}{R}$

i.e., $\mathbf{i_L} = \frac{\boldsymbol{v_i}}{\boldsymbol{R}}$

i.e., i/p voltage v_i is converted to current $\frac{v_i}{R}$.

Thus, the circuit acts as a voltage to current convertet.

Applications of V-I Converters:

- Low voltage (0 to 1 V) DC and AC voltmeters.
- LED and Zener diode tester

Current to Voltage (I to V) Converter

(or Transresistance amplifier)

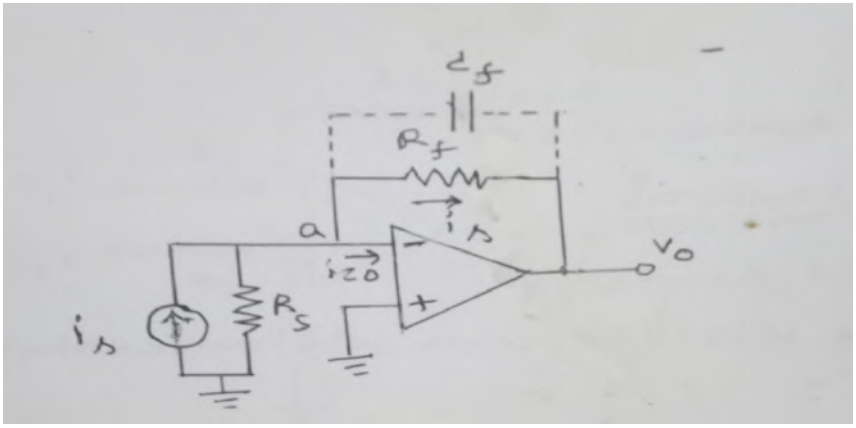


Fig. 6 (c): I to V converter

Fig. 6 (c)shows an I to V converter.

Let us assume virtual ground at the i/p of opamp. Then, no current flows through R_S. i.e., i_s flows through R_f.

From Fig. 6 (c), we write

$$i_s = \frac{v_a - v_o}{R_f} \quad \ldots\ldots\ldots (1)$$

Due to virtual ground, $v_a = 0$

$\therefore$ Eq. (1) becomes $i_s = \frac{-v_o}{R_f}$

i.e., $\boldsymbol{v_o = -i_s R_f}$

i.e., i/p current is converted to an o/p voltage v_o.

Here, resistor R_f is shunted by a capacitor C_f to reduce high frequency noise and possibility of oscillations.

Instrumentation Amplifier

Instrumentation Amplifiers are widely used in instrumentation and control systems. They are especially used to amplify the low output of transducers.

Derivation for the output of an Instrumentation Amplifier:

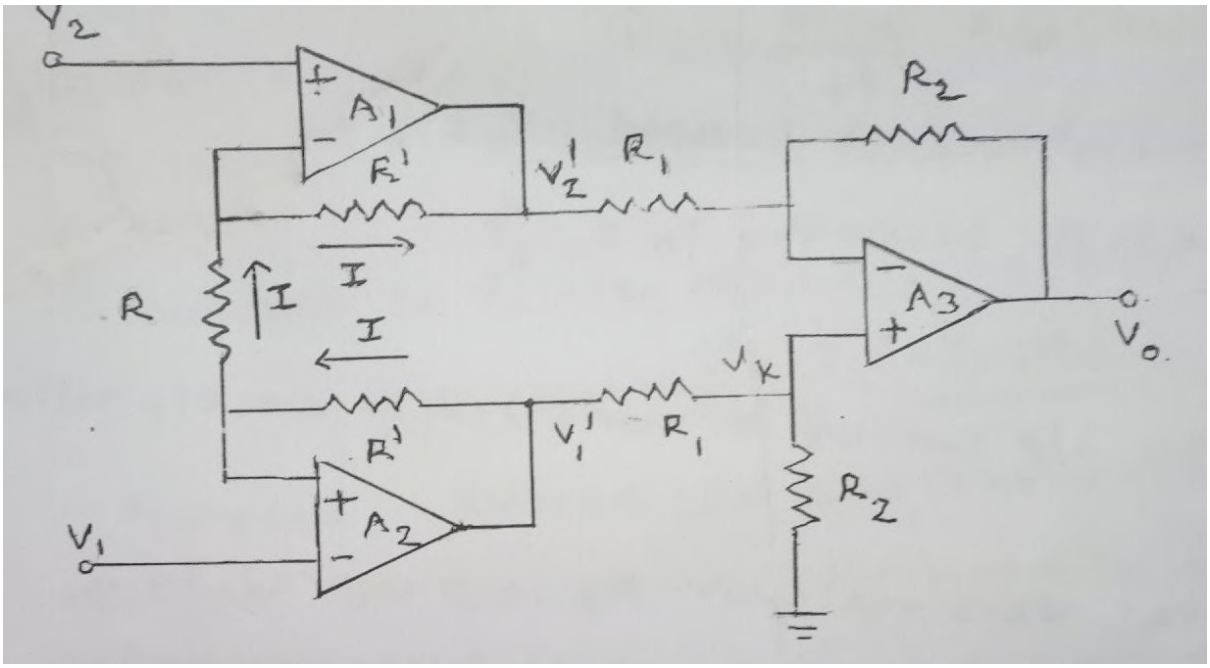


Fig. 7 (a): Instrumentation Amplifier

Fig. 7(a) shows an instrumentation amplifier using 3 opamps A_1, A_2 and A_3.

The circuit for A_3 as shown in the Fig. 7 (b).

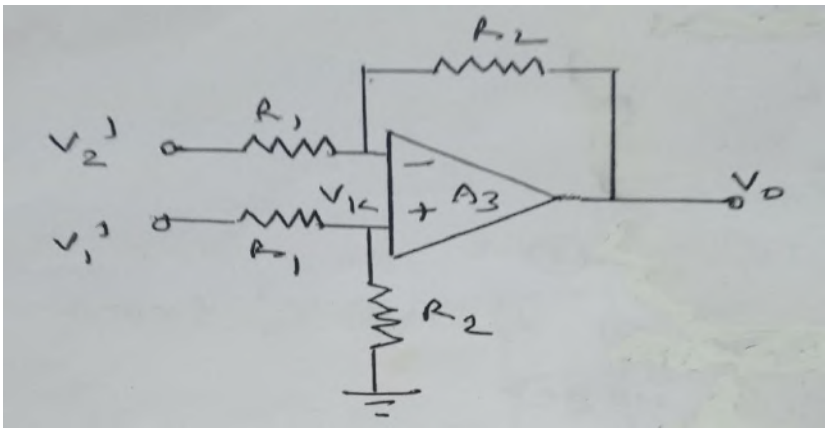


Fig. 7 (b)

Fig. 7 (b) represents a subtractor (i.e., a difference amplifier)

Let V_k be the voltage at the (+) terminal of A_3. Then

$$V_k = V_1' \cdot \frac{R_2}{R_1+R_2} \quad \ldots\ldots (1)$$

By applying super position theorem, we get

$$V_o = V_k \left(1 + \frac{R_2}{R_1}\right) + V_2' \left(\frac{-R_2}{R_1}\right)$$

$$= V_k \left(\frac{R_1+R_2}{R_1}\right) - V_2' \frac{R_2}{R_1}$$

Putting the value of V_k from eq. (1) in to above equation, we get

$$V_o = V_1' \frac{R_2}{\cancel{R_1+R_2}} \frac{\cancel{R1+R2}}{R_1} - V_2' \frac{R_2}{R_1}$$

Thus $\frac{R_2}{R_1}(V_1' - V'_2)$ ..... (2).

Let opamp be ideal. i.e., no current flows through any input terminal of opamp. Voltage at (-) terminal = V_2 and vo(+) terminal = V_1

So, current I flowing upwards through R_1 is

$$I = \frac{V_1-V_2}{R} \ldots\ldots (3)$$

From the circuit, we can write

$$I = \frac{V_1' - V_1}{R}$$

i.e., $V_1' - V_1 = IR'$

or $$V_1' = V_1 + IR' \ldots\ldots (4)$$

Similarly

$$I = \frac{V_2 - V_2'}{R'}$$

Or $V_2 - V_2' = IR'$

i.e., $V_2' = V_2 - IR'$ …… (5)

Substituting the values of V_1' and V_2' from eqs. (4) and (5) in eq. (2), we get

$$Vo = \frac{R_2}{R_1}(V_1 + IR' - V_2 + IR')$$

$= \frac{R_2}{R_1}(V_1 - V_2 + 2IR')$ ……. (6)

Putting the value of 'I' from eq. (3) into eq. (6), we get

$$Vo = \frac{R_2}{R_1}[(V_1 - V_2) + 2\frac{R'}{R}(V_1 - V_2)]$$

i.e., $\mathbf{Vo = \frac{R_2}{R_1}(V_1 - V_2)\ [1 + 2\frac{R'}{R}]}$ …… (7)

Important points about R:

(i) Differential gain of this amplifier can be varied by varying R. So replace R with a variable resistor (Potentiometer)

(ii) If we use potentiometer, and if we put the wiper to lower side, then R may become zero. So, Vo becomes ∞.

(iii) So, we connect a fixed resistor (e.g.: 1 KΩ) in series with potentiometer. So, we will get a minimum value of R = 1 KΩ. Thus, the problem in (ii) can be avoided.

Differentiator

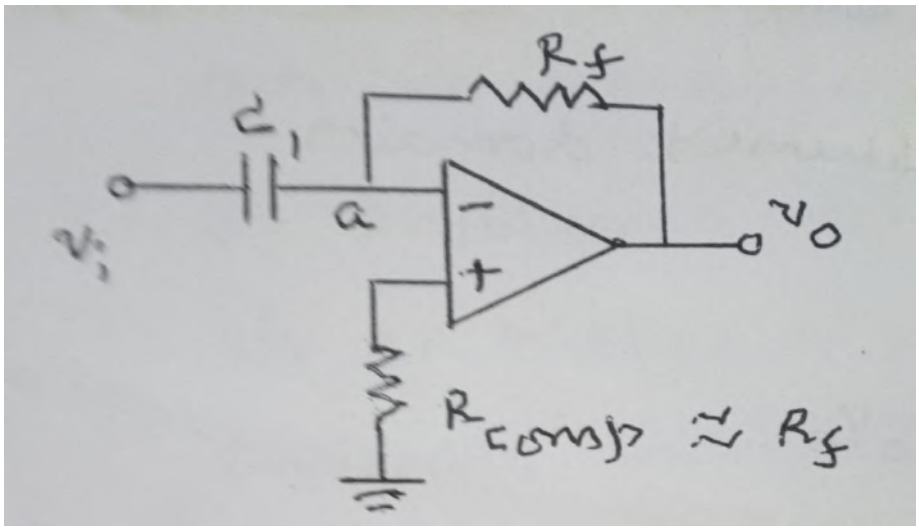


Fig. 8 (a) Ideal Differentiator

Differentiator is a Circuit whose output is directly proportional to the derivative of input.

(a) Differentiator

Fig. 8 (a) represents adifferentiator circuit. Consider node 'a'.

Nodal equation at node 'a' is

$$C_1 \frac{d(v_a - v_i)}{dt} + \frac{v_a - v_o}{R_f} = 0 \quad \ldots\ldots (1)$$

For ideal opamp, there exists a virtual ground at the input of the opamp.

i.e., $v_a = 0$

∴Eq. (1) becomes $-C_1 \frac{dv_i}{dt} = \frac{v_o}{R_f}$

or $\boldsymbol{v_o = -R_f C_1 \frac{dv_i}{dt}}$

i.e., v_o is directly proportional to $\frac{dv_i}{dt}$, where R_fC_1 is a proportionality constant. So, it is a differentiator circuit.

(b) Analysis in the frequency domain:

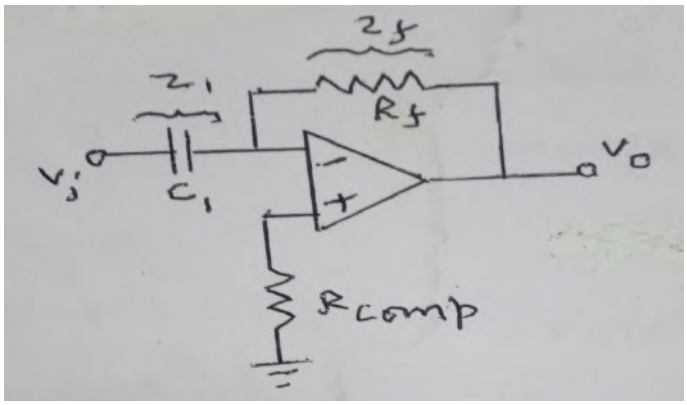


Fig. 8 (b)

Consider Fig. 8 (b).

$Z_1 = \frac{1}{sC_1}$

$Z_2 = R_f$

Gain A(s) $= -\frac{Z_f}{Z_1}$

$= \frac{R_f}{1/sC_1}$

$= - sR_fC_1$ ..... (1)

$= - jw R_fC_1$ ($\because s = j \omega$)

$= - j2\pi fR_fC_1$

$= - j f/(1/2\pi R_fC_1)$

$= - j f/f_a$

$|A| = \frac{f}{f_a}$

where $\boldsymbol{f_a} = \frac{\mathbf{1}}{\mathbf{2\pi R_f C_1}}$

At f = f_a , | A | = 1. i.e., 0 dB and gain increases at + 20 dB/decade.

(c) Problems with ideal differentiator:

(i) At higher frequencies, it may become instable and result in oscillations.

(ii) Input impedance (= 1/ ωC_1) decreases with increase in frequency. Thus, the circuit becomes sensitive to high frequency noise.

To avoid above problems, we use practical differentiator circuit.

(c) Practical Differentiator:

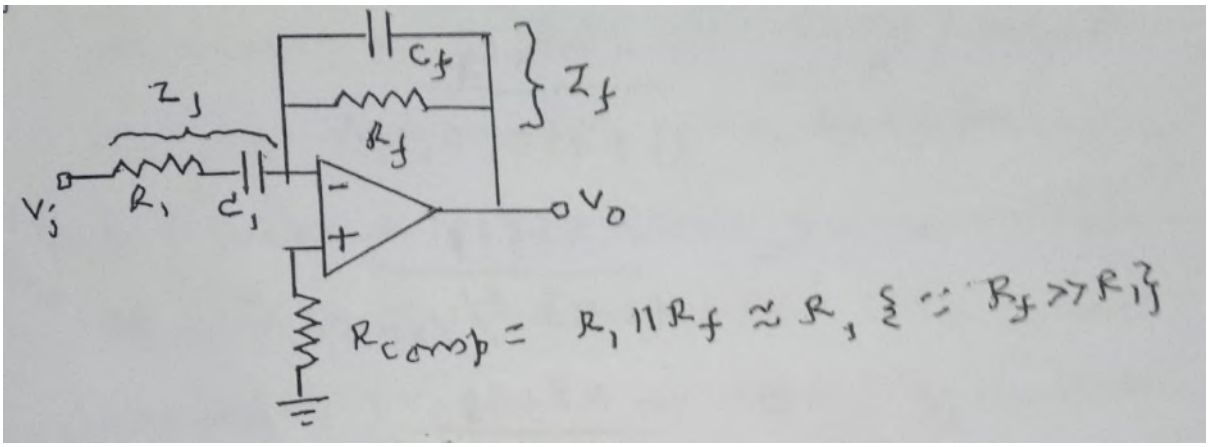


Fig. 8 (c) Practical differentiator circuit

Fig. 8 (c) represents a practical differentiator circuit. From figure, we write

$$Z_1 = R_1 + \frac{1}{sC_1} = \frac{1+sR_1C_1}{sC_1} \quad \ldots\ldots \quad (1)$$

$$Z_f = R_1 \| \frac{1}{sC_f} = \frac{R_f \cdot \frac{1}{sC_f}}{R+\frac{1}{sC_f}}$$

$$= \frac{R_f}{1+sR_fC_f} \quad \ldots\ldots\ldots \quad (2)$$

We know that $A = -\frac{Z_f}{Z_1}$

$$= -\frac{R_f}{1+sR_fC_f} \cdot \frac{sC_1}{1+sR_1C_1} \quad \{\text{from eqs. (1) and (2)}\}$$

$$= -\frac{sR_fC_1}{(1+sR_fC_f)(1+sR_1C_1)}$$

If $R_fC_f = R_1C_1$,

above equation becomes

$$A = \frac{-sR_fC_1}{(1+sR_1C_1)^2} \quad \ldots\ldots\ldots (3)$$

At steady state, $s = j\omega = j.2\pi f$

∴ Eq. (3) becomes

$$A = \frac{-sR_fC_1}{(1+j2\pi fR1C1)^2}$$

$$= \frac{-sR_f C_1}{\left\{1+jf \ / \ (\frac{1}{2\pi fR1C1})\right\}^2}$$

$$= \frac{-sR_f C_1}{\{1+jf \ / \ f_b\}^2}$$

Where $\mathbf{f_b} = \frac{\mathbf{1}}{\mathbf{2\pi R_1 C_1}}$

(d) Frequency Response of Differentiator:

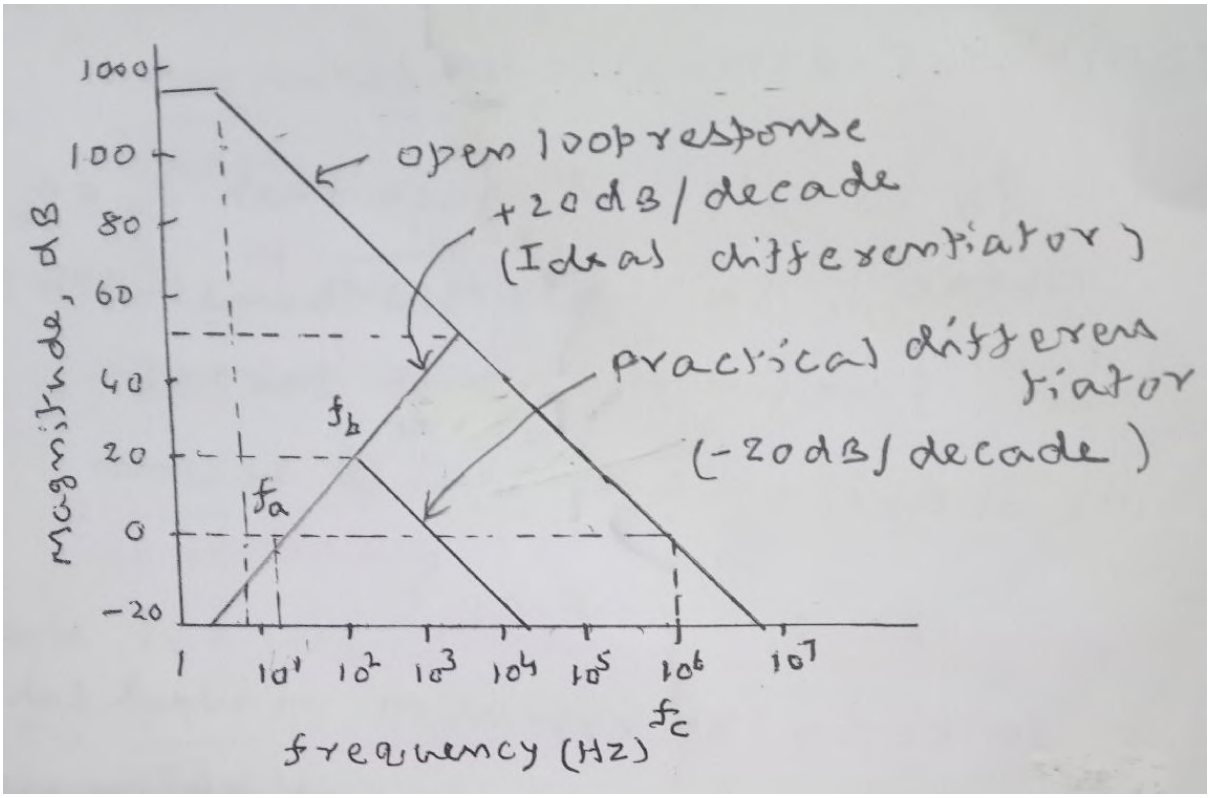


Fig. 8 (d) Frequency response of ideal and practical differentiator

Fig. 8 (d) represents the frequency response of ideal and practical differentiators.

*When $f < f_b$, gain increases at a rate of 20 dB/decade.

*When $f > f_b$

- For practical differentiator, gain decreases at a rate of − 20 dB/decade. This is due to R_1C_1 and R_fC_f factors.
- For ideal differentiator, gain increases at a rate of 20 dB/decade. This causes stability problems at high frequencies

(e) Other practical considerations:

(i) f_b is selected such that $f_a < f_b < f_c$, where f_c is unity gain bandwidth (UGB), i.e., frequency at which gain = 1.

(ii) If $R_fC_1 \gg R_1C_f$ (orR_fC_f), eq. (3) becomes

$$A = -sR_fC_1$$

which is the expression in ideal case.

(iii) If 'T' is the time period of input signal, it is selected such that

$T \gg R_fC_1$

(iv) A resistorR_{Comp}(= $R_1 \| R_f$) is connected to the non-inverting terminal to compensate for the effect of input bias current.

(f) Design Procedure:

* Choose f_a = highest frequency of input signal.

f_a is given by $f_a = \frac{1}{2\pi R_f C_1}$

* Let $C_1 < 1$ μF (say C1 = 0.1 μF) and calculate $R_f$from the above formula.

* Choose $f_b = 10\ f_a$ (say) and calculate the values of R_1

f_b is given by $f_b = \frac{1}{2\pi R_1 C_1}$

* Find C_f such that $R_1C_1 = R_fC_f$

Problem 2.4:

Design an opamp differentiator that differentiates an input signal with frequency = 100 Hz

Solution:

(a) $f_a = f_{max} = 100$ MHz

i.e., $\frac{1}{2\pi R_f C_1} = 100$ or i.e., $R_f = \frac{1}{2\pi\ x\ 100\ x\ C1}$

Choose C1 = 0.1 μF10^{-6}

$\therefore R_f = \frac{1}{2\pi\ x\ 100\ x\ 0.1\ x\ 10^{-6}} = 15.9$ KΩ

Now choose $f_b = 10\ f_a = 10$ x 100 = 1000Hz

i.e., $\frac{1}{2\pi R_1 C_1} = 1000$

$\therefore R_1 = \frac{1}{2\pi \ x \ 1000 \ x \ C1}$

$= \frac{1}{2\pi \ x \ 1000 \ x \ 0.1 \ x \ 10^{-6}} = 1.59 \ K\Omega$

Since $R_f c_f = R_1 C_1$

$C_f = \frac{R_1 C_1}{R_f} = \frac{1.59 \ x \ 10^3 \ x \ 0.1 \ x \ 10^{-6}}{15.9 \ x \ 10^3}$ 0.01 μF

Integrator

Integrator is a circuit whose output is directly proportional to the time integral of input voltage.

(a) Integrator:

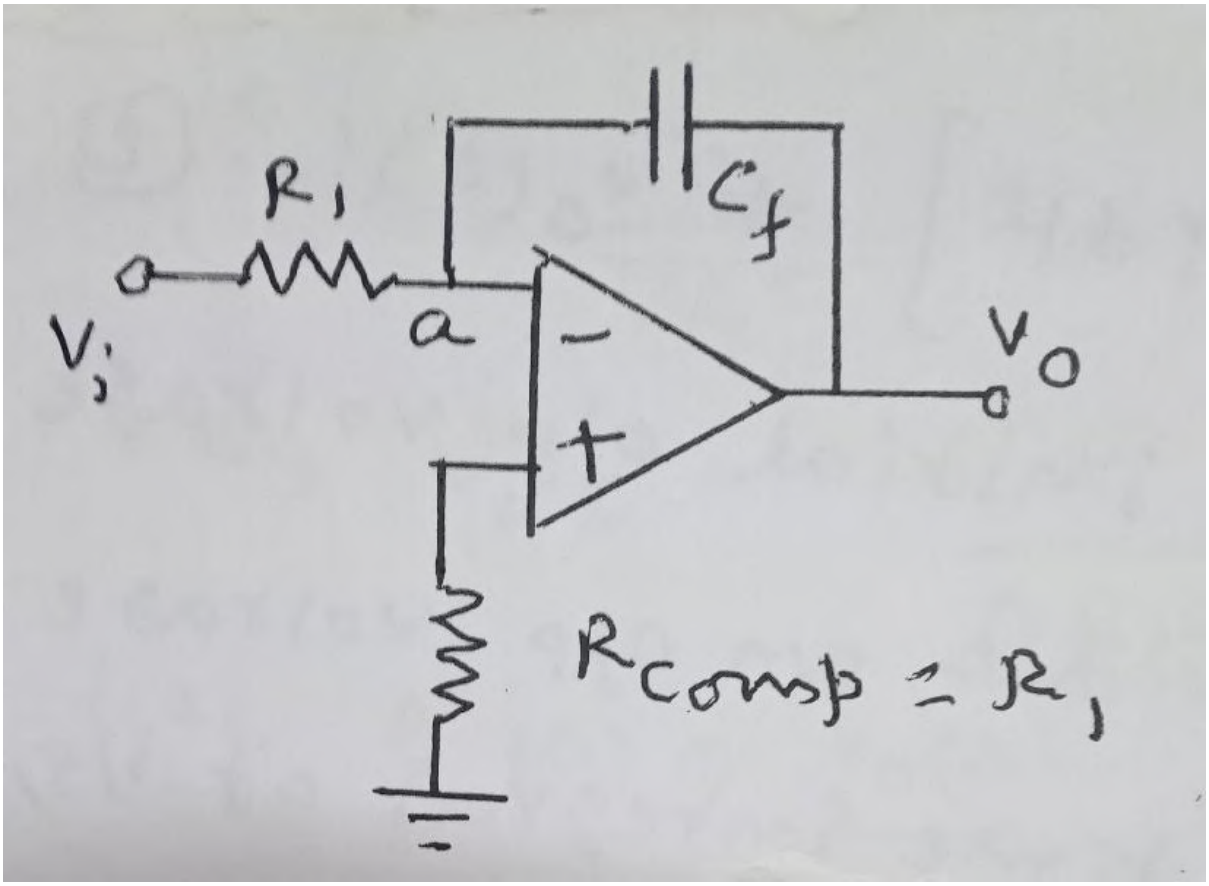


Fig. 9 (a) Integrator

Fig. 9 (a) represents an opamp integrator. Consider node 'a'. Nodal equation at node 'a' is

$$\frac{v_a - v_i}{R_1} + C_f \frac{d(v_a - v_o)}{dt} = 0 \quad \ldots\ldots (1)$$

For an ideal opamp, there exists a virtual ground at the input of the opamp.

i.e., $v_a = 0$

∴ Eq. (1) becomes

$-\frac{v_i}{R_1} - C_f \frac{dv_o}{dt} = 0$

i.e., $C_f \frac{dv_o}{dt} = -\frac{v_i}{R_1}$

or $\frac{dv_o}{dt} = \frac{-1}{R_1 C_f} v_i$

or $dv_o = -\frac{1}{R_1 C_f} v_i \, dt$

Integrating above equation on both sides, we get

$$\boldsymbol{v_o = \left[\frac{-1}{R_1 C_f} \int_0^t v_i \, dt\right]} + v_o(0) \quad \ldots. (2)$$

where v_o (0) is the initial o/p voltage.

Thus, the circuit provides an o/p voltage proportional to the time integral of i/p voltage. So, it is called an integrator. circuit. Here R_1C_f is the time constant of integrator.

R_{Comp} is called compensating resistor. It is connected to the non-inverting terminal of opamp to minimize the effect of input bias current on o/p voltage.

(b) Analysis in the frequency domain:

Nodal equation at node 'a'is

$\frac{v_a - v_i}{R_1} + C_f \frac{d(v_a - v_o)}{dt} = 0$

In frequency domain, it is

$\frac{v_a - v_i}{R_1} + \frac{v_a - v_o}{1/sC_f} = 0 \quad \ldots \quad (1)$

Because of virtual ground $v_a = 0$

∴ Eq. (1) becomes

$-\frac{v_i}{R_1} - \frac{v_o}{1/sC_f} = 0$

$i.e., \frac{v_o}{1/sC_f} = \frac{v_i}{R_1}$

$i.e., v_o = -\frac{v_i}{sR_1C_f} \quad \ldots \quad (2)$

$$A(s) = \frac{v_o(s)}{v_i(s)} = -\frac{1}{sR_1C_f} \quad \ldots (3)$$

In steady state, s = j ω

∴ Eq. (3) becomes

$$A(j\omega) = -\frac{1}{j\omega R_1 C_f} \text{ (Since } 1/j = -j)$$

$$|A(j\omega)| = \frac{1}{\omega R_1 C_f}$$

$$= \frac{1}{2\pi f_b R_1 C_f} \quad \ldots (4)$$

When gain = 1 (i.e., 0 dB) , eq.(4) becomes

$$\frac{1}{2\pi f_b R_1 C_f} = 1$$

Or $$\mathbf{f_b = \frac{1}{2\pi R_1 C_f}}$$

(c) Problem at low frequencies

At low frequencies or atdc frequencies, $f_b = 0$. So, C_f behaves as an open circuit. So, there is no – ve feedback. i.e., opamp operates in open loop. i.e., gain is infinite. This can be verified by putting $f_b = 0$ in eq. (4), where we get $|A| = \infty$.

In practice, gain doesn't become infinity because o/p saturates at a value $\pm V_{Sat}$, which is closer to supply voltage. But we do not want even this high gain.

Solution to this problem is a practical integrator circuit.

(d) Practical Integrator Circuit (or lossy integrator)

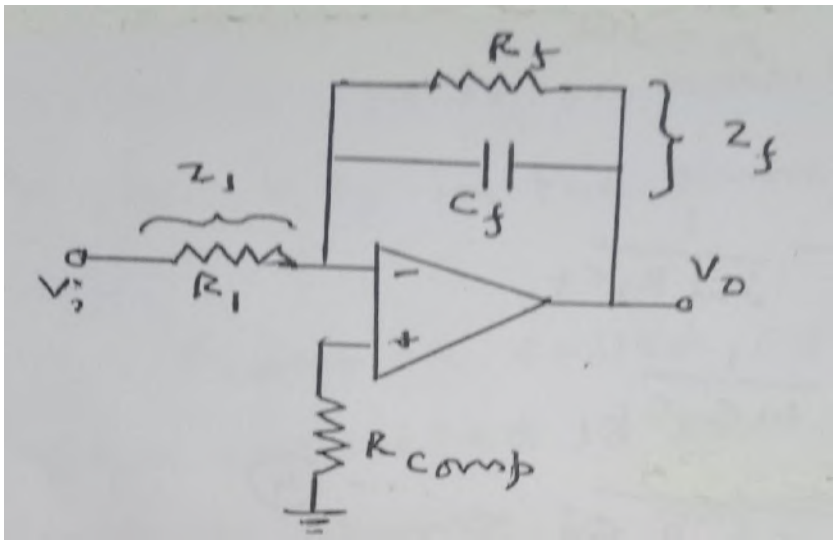


Fig. 9 (b) Practical Integrator

Fig. 9 (b) represents a practical integrator circuit. Since parallel combination of R_f and C_f dissipates some power, the circuit is also called lossy integrator.

From the circuit, we write

$Z_1 = R_1$

$$Z_f = R_1 \| \frac{1}{sC_f} = \frac{R_f \cdot \frac{1}{sC_f}}{R + \frac{1}{sC_f}}$$

$$= \frac{R_f}{1 + sR_fC_f}$$

But $\frac{v_o(s)}{v_i(s)} = -\frac{Z_f}{Z_1}$

$$= -\frac{R_f}{R_1(1 + sR_fC_f)}$$

$$= \frac{-R_f/R_1}{1 + j\omega R_fC_f} \quad \ldots\ldots\ldots (1)$$

$$= \frac{-R_f/R_1}{1 + j2\pi\omega R_fC_f}$$

$$= \frac{-R_f/R_1}{1 + jf / (\frac{1}{2\pi f R_fC_f})}$$

$$= \frac{-R_f/R_1}{\{1 + jf / f_a\}^2}$$

Where $f_a = \frac{1}{2\pi R_fC_f}$

Eq. (1) $\Rightarrow A|jw| = \frac{R_f/R_1}{\sqrt{1 + \omega^2 R_f^2 C_f^2}}$ ……(2)

(e) Frequency response

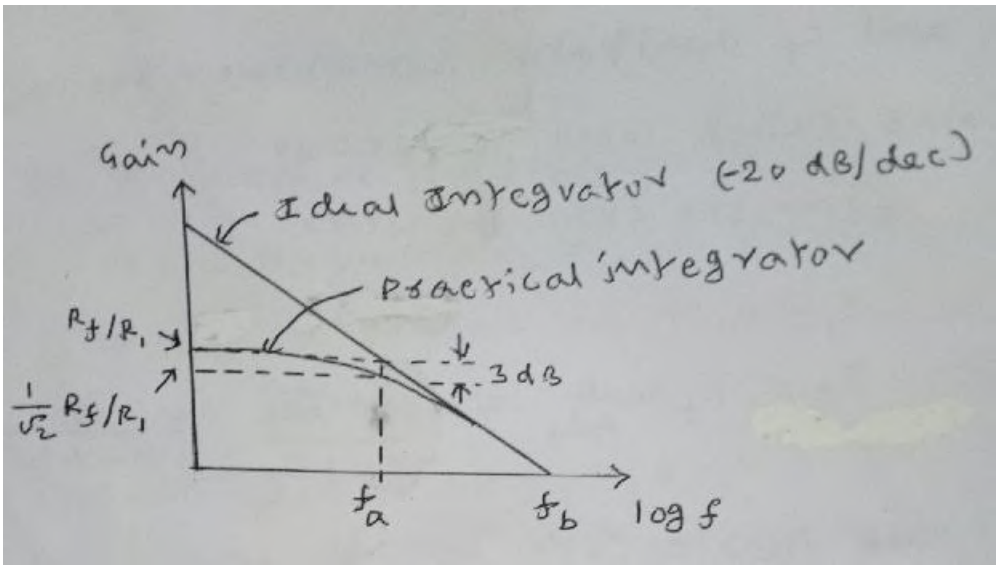


Fig. 9 (c) Frequency response of ideal and practical integrators

Fig. 9 (c) represents the frequency response of ideal and practical integrators

Ideal case: Here graph is a straight line with a slope of -20 dB/decade. f_b is the frequency at which the gain of integrator is 0 dB

$f_b = \frac{1}{2\pi R_1 C_f}$

Practical case:

At f = 0,

| A | = R_f / R_1 (see graph)

f_a is corner frequency. i.e., frequency at which the gain is 0.707 R_f / R_1 or – 3 dB below R_f / R_1

At f = fa,

Gain = .707 $\frac{R_f}{R_1} = \frac{1}{\sqrt{2}} . \frac{R_f}{R_1}$ (Since $\frac{1}{\sqrt{2}}$ = .707)

i.e., $\frac{Rf / R1}{\sqrt{1+\omega^2 R^2 C^2}} = \frac{1}{\sqrt{2}} . \frac{R_f}{R_1}$

i.e., $1 + \omega^2 {R_f}^2 {C_f}^2 = 2$

i.e., $\omega^2 {R_f}^2 {C_f}^2 = 2\text{-}1 = 1$

i.e., $\omega R_f C_f = 1$

i.e., $2\pi f_a R_f C_f = 1$

i.e., $f_a = \frac{1}{2\pi R_f C_f}$

(f) Practical considerations:

* If frequency f < f_a, there is no integration. i.e., Circuit behaves like a simple inverting amplifier.

* If f = f_a, accuracy is 50%.

* If f = 10 f_a, accuracy is 99%.

AC Amplifier

Generally, opamp amplifies DC as well as AC signals. If we want only AC amplification, we should block DC signals. This is achieved by using capacitors, because a capacitor blocks DC signals.

(a) Inverting AC amplifier:

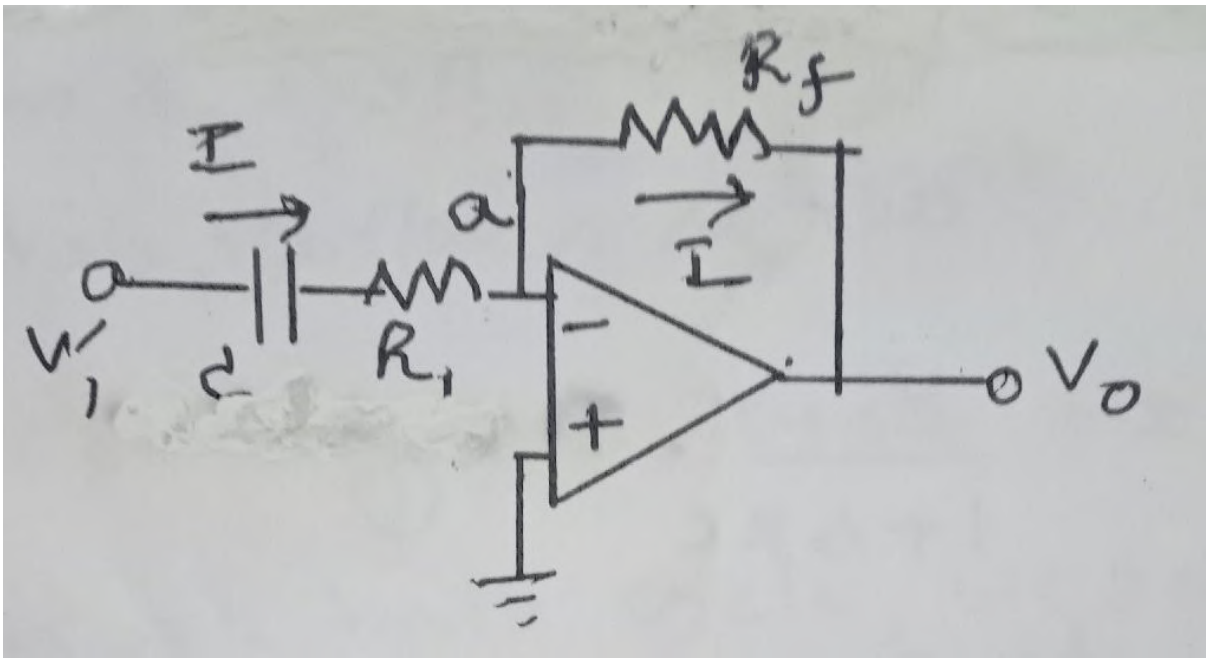


Fig. 10 (a) Inverting AC follower

Fig. 10 (a) represents an inverting AC amplifier. capacitor C blocks DC component. Resistor 'R_1' and Capacitor 'C' set the lower 3 dB frequency of the amplifier.

Consider node 'a'.

Nodal equation at node 'a' is

$\frac{v_a - v_i}{R_1 + \frac{1}{sC}} + \frac{v_a - v_o}{R_f} = 0$ ….. (1)

Due to virtual ground for ideal opamp,

$v_a = 0$

∴ Eq. (1) becomes

$$\frac{-v_i}{R_1+\frac{1}{sC}} = \frac{v_o}{R_f}$$

$$\therefore \text{ A}_{\text{CL}} = \frac{v_o}{v_i} = \frac{-R_f}{R_1+\frac{1}{sC}}$$

In the midband, C acts as a short circuit. i.e., $\frac{1}{\omega C} = 0$

(b) Non-inverting AC amplifier:

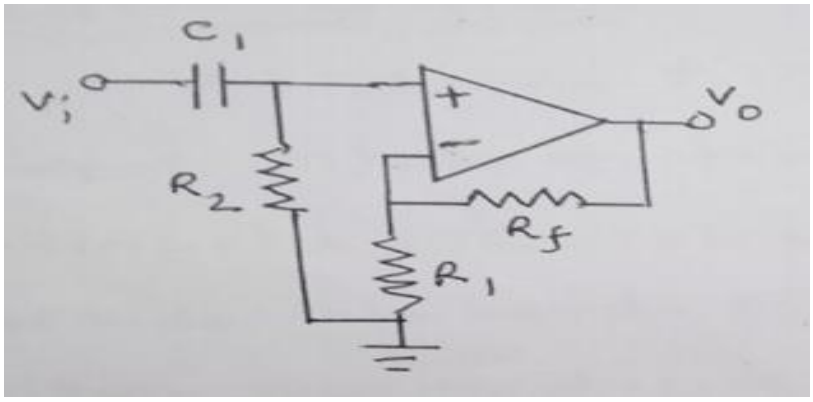


Fig. 10 (b) non-inverting AC amplifier

Fig. (b) shows a non-inverting AC amplifier. Here, R_2 is added to provide a DC return path to ground.

AC Voltage Follower:

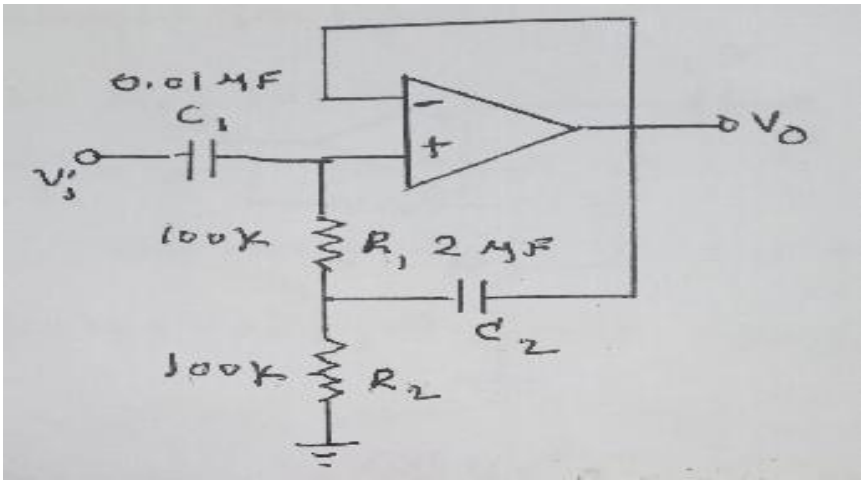


Fig. 10 (c) AC Voltage follower

Fig. 10 (c) shows a practical AC voltage follower circuit. Capacitors C_1 and C_2 are chosen high so that they act as short circuits at all frequencies of operation.

Resistors R_1 and R_2 provide a path for DC current in to the (+) terminal of opamp.

C_2 acts as a boot strapping capacitor and connects R_1 to v_o for AC operation. Hence the input resistance seen by the source $\approx \frac{R_1}{1-A_{CL}}$ (from Miller's theorem), where A_{CL} is closed circuit voltage gain of the circuit. (≈1)

Thus, high input impedance can be obtained.

NON-LINEAR APPLICATIONS OF OP-AMP

COMPARATORS

A comparator is a circuit which compares a signal voltage applied at one i/p of opamp with a known reference voltage at the other input. It is basically an open loop opamp with output ± V_{SAT}, where V_{SAT} is the saturation voltage of opamp. Comparators are classified as non-inverting and inverting comparators.

(a) Non-Inverting Comparators.

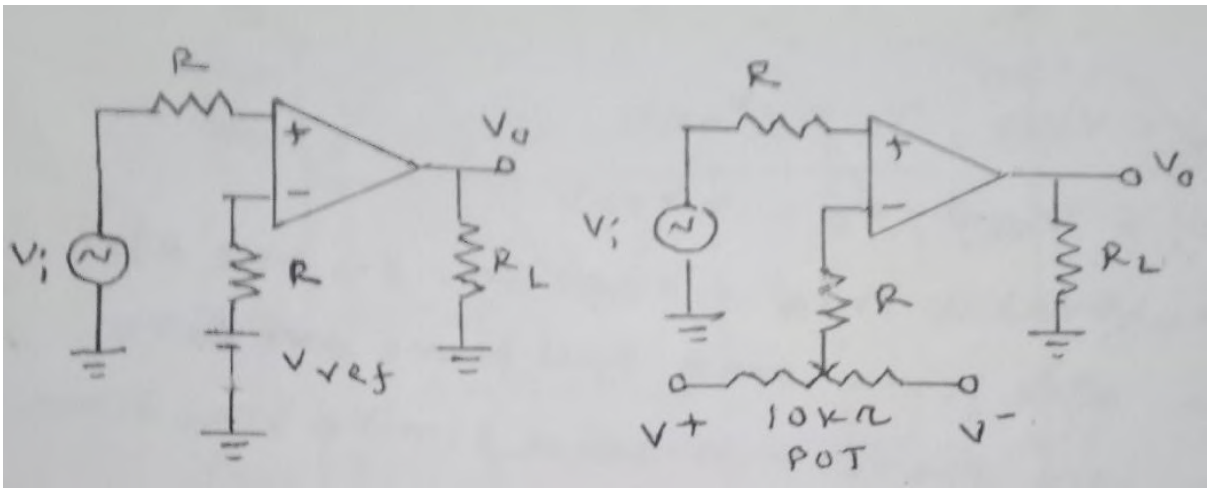


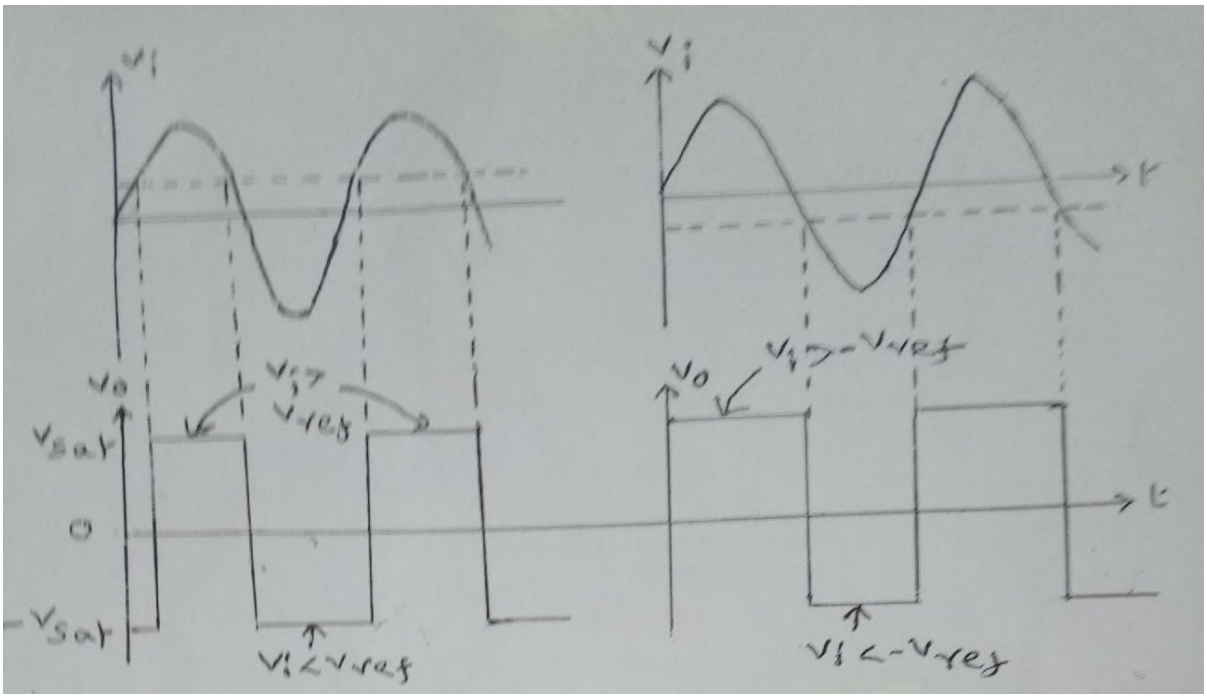
Fig. 1 (a) Non-inverting Comparator **Fig. 1 (b) Practical Circuit**

Fig. 1(a) shows a non-inverting comparator. A fixed reference voltage V_{ref} is applied at (-) terminal of opamp and a time varying voltage v_i is applied at (+) terminal. In a practical circuit, V_{ref} is obtained by connecting a 10 KΩ potentiometer which forms a voltage divider with supply voltagesV^+ and V^- as shown in Fig. 1 (b).

When $v_i < V_{ref}$, $v_o = -V_{Sat}$

When $v_i > V_{ref}$, $v_o = +V_{Sat}$

Fig. 2 illustrates this situation. In the o/p waveforms, rise time and fall time are zero. Butpractically there will be a finite rise time and fall time. i.e., o/p of comparator cannot change suddenly and sharply.



(b) Inverting Comparator:

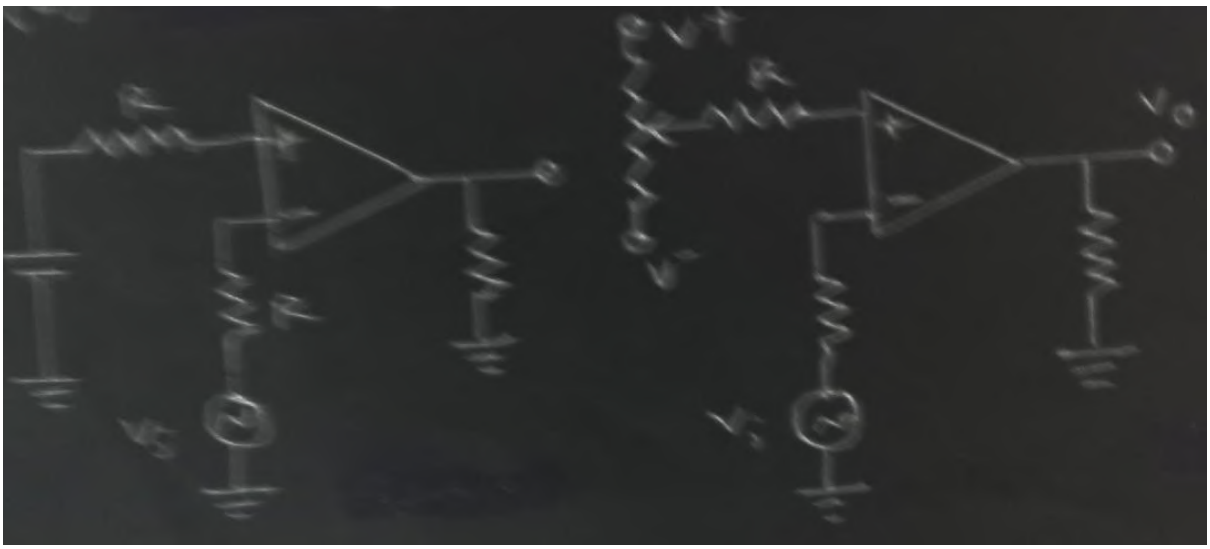


Fig. 3 (a) Inverting Comparator **Fig. 3 (b) Practical circuit**

Fig. 3(a) shows an inverting comparator. v_i is applied to the inverting terminal of opamp and constant reference voltage V_{ref} is applied to the non-inverting terminal.

In a practical circuit shown in Fig. 3(b), a 10 KΩ potentiometer is used to obtain V_{ref}. It forms a voltage divider with supply voltages V^+ and V^-.

When $v_i <$ Vref, $v_o = + V_{Sat}$

When $v_i >$ Vref, $v_o = - V_{Sat}$

as shown in Fig. 4 (a) and 4 (b)

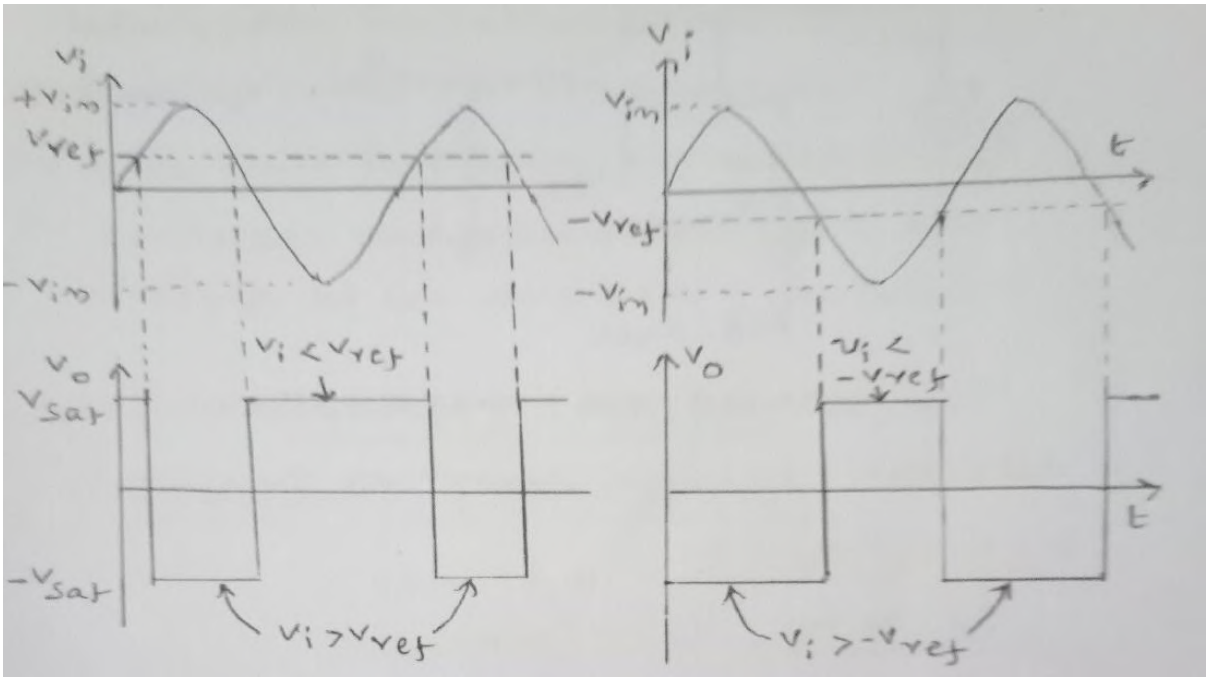


Fig. 4 (a) Fig. 4 (b)

Applications of comparators:

- Zero-crossing detector
- Window detector
- Time Marker Generator
- Phase meters
- Schmitt Tigger
- Oscillators

<u>Zero Crossing Detector:</u>

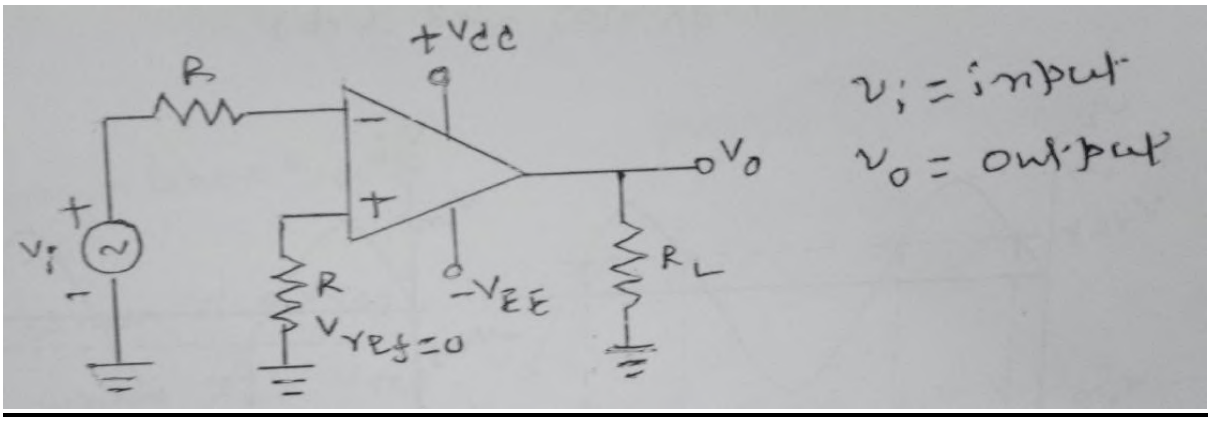


Fig. 5 (a) shows an inverting zero-crossing detector. It is an inverting comparator, where V_{ref} = 0

If $v_i > 0$, $v_o = -V_{Sat}$

If $v_i < 0$, $v_o = +V_{Sat}$

Whenever $v_i = 0$, v_o changes its state. Its i/p and o/p waveforms are shown in Fig. 5 (b).

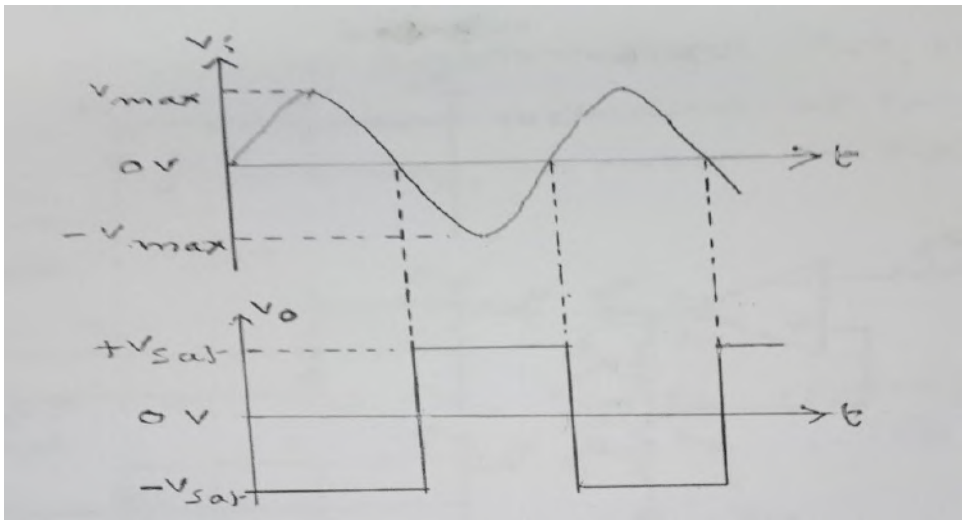


Fig. 5 (b)

Applications of Zero-crossing Detector:

(i) Used as Time Marker Generator

(ii) Sine wave to square wave generator

(iii) To detect and count multiple zero-crossings of an arbitrary waveform.

SCHMITT TRIGGER

(orRegenerative Comparator)

Schmitt Trigger is a comparator circuit with regenerative (i.e., + ve) feedback. Because of + ve feedback, gain increases and transfer curve becomes closer to ideal curve.

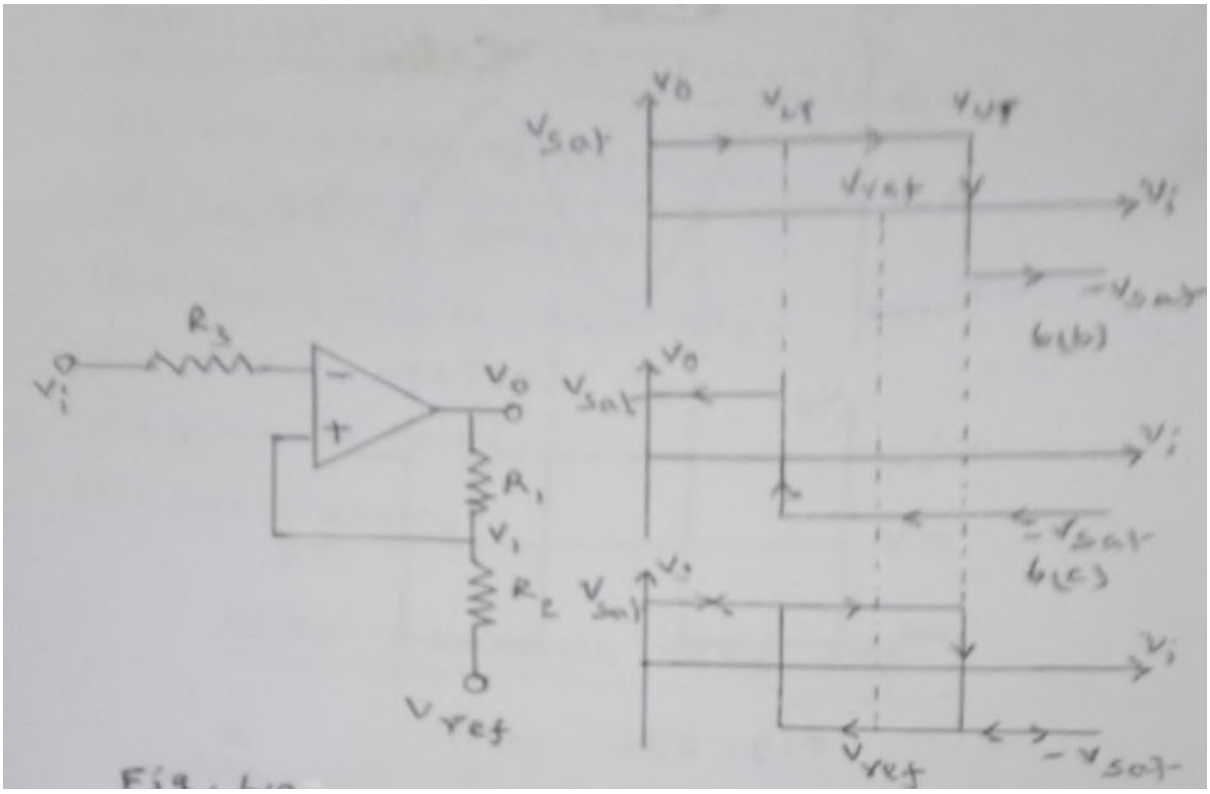


Fig. 6 (a) Fig. 6 (b), (c) and (d

Fig. 6 (a) shows an inverting Schmitt Trigger. Let v_i be the i/p and vo be the o/p voltage of the circuit.

v_i triggers v_o every time it exceeds certain voltage levels. These voltage levels are called **"Upper Threshold Voltage (V_{UT})"** and **"Lower Threshold Voltage (V_{LT})".**

(V_{UT} - V_{LT}) is called **"Hysteresis Width (V_H)".**

Let v_o = + $V_{Sat.}$

Then,the voltageat the + terminal is obtained by Superposition theorem as

$$V_1 = V_{UT} = \frac{V_{ref}\,R_1}{R_1+R_2} + \frac{R_2 v_o}{R_1+R_2}$$

$$= \frac{R_1 V_{ref}}{R_1+R_2} + \frac{V_{Sat}\,R_2}{R_1+R_2} \quad \ldots\ldots. (1) \quad (\text{Since } v_o = + V_{Sat.})$$

As long as $v_i < V_{UT}$, v_o remains $+V_{Sat}$.

When v_i is just greater than V_{UT}, the o/p switches to - V_{Sat}

and remains at this level as long as $v_i > V_{UT}$ as shown in Fig. 6 (b)

When v_o = - V_{Sat}

$V_1 = V_{LT} = \frac{V_{ref}\, R_1}{R_1 + R_2} + \frac{v_o R_2}{R_1 + R_2}$

$= \frac{V_{ref}\, R_1}{R_1 + R_2} - \frac{V_{Sat}\, R_2}{R_1 + R_2}$ $(\because v_o = - V_{Sat})$ ……. (2)

Eqs. (1) and (2) ⇒

Hysteresis Width $V_H = V_{UT} - V_{LT}$

$= \frac{2\, V_{Sat}\, R_2}{R_1 + R_2}$ ……. (3)

When v_i is just $<V_{LT}$, v_o switches from $- V_{Sat}$ to $+ V_{Sat}$. Fig. 6 (c) shows this regenerative transition.

Fig. 6 (d) shows composite (complete) transfer characteristics and illustrates hysteresis loop.

Important Points:

(i) Because of hysteresis, the circuit triggers at higher voltage for increasing signals than for decreasing signals.

(ii) V_H is independent of V_{ref}. {See eq. (3). There is no Vref term.}.

(iii) R_3 is chosen equal to $R_1 \| R_2$ to compensate for input bias current.

(iv) A non-inverting Schmitt Trigger is obtained by interchanging v_i and V_{ref}.

(v) The most important application of Schmitt Trigger is to convert a very slowly varying i/p voltage into a square wave o/p.

Problem 2.5: In the circuit of the Schmitt Trigger shown in Fig. 6 (a), R_1 = 50 KΩ, R_2 = 100 KΩ, V_{ref} = 0 V, v_i = 1 V_{pp} (peak-to-peak) sine wave and saturation voltage = ± 14 V. Determine upper and lower threshold voltages. Also calculate hysteresis width.

Solution:

Given that R_1 = 50 KΩ, R_2 = 100 KΩ, V_{ref} = 0 V, v_i = 1 V_{pp} (peak-to-peak) sine wave.

Upper Threshold Voltage $V_{UT} = \frac{R_1 V_{ref}}{R_1 + R_2} + \frac{V_{Sat}\, R_2}{R_1 + R_2}$

$= 0 + \frac{V_{Sat}\, R_2}{R_1 + R_2}$ $(\because V_{ref} = 0)$

$= \frac{14\ x\ 100}{50000\ + 100}$ = 28 mV

Lower Threshold Voltage $V_{LT} = 0 - \frac{V_{Sat}\, R_2}{R_1 + R_2}$

$$= - \frac{14\ x\ 100}{50000 + 100} = - 28\ V$$

Hysteresis width $V_H = V_{UT} - V_{LT}$

$= 28\ mV - (- 28\ mV) = 56\ mV$

SQUARE WAVE GENERATOR

(or ASTABLE MULTIVIBRATOR)

A square wave generator is also called astable multivibrator or free running oscillator. It is shown in Fig. 7 (a). Here opamp operates in saturation region. Fig. 7 (b) show the waveforms for v_o and v_c, where v_o is o/p of the circuit and v_c is voltage across capacitor C. Let the voltage at (+) terminal of opamp be V_{ref}.

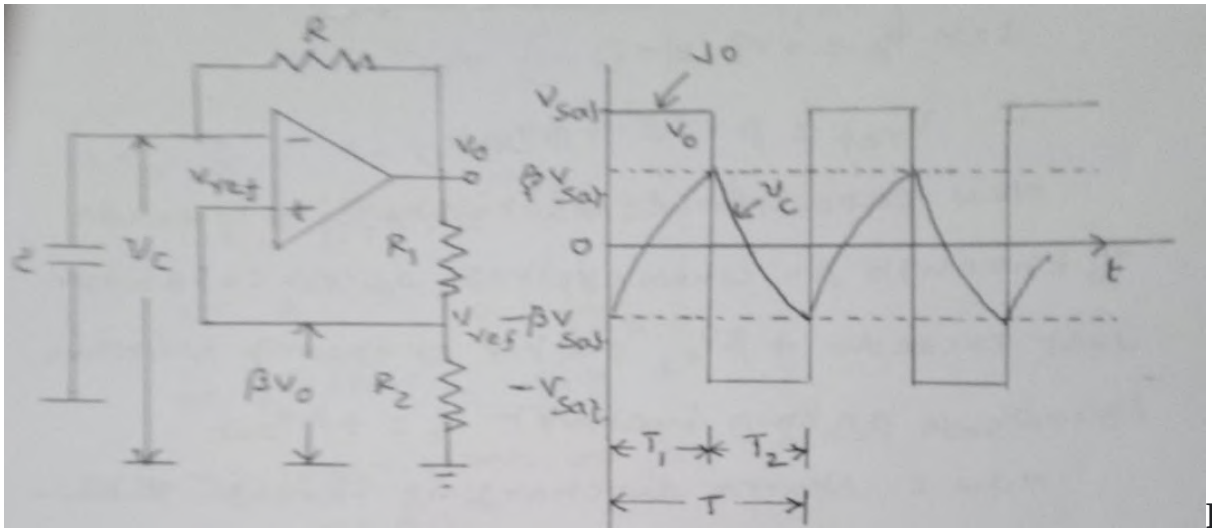


Fig. 7(a) Square wave Generator

A fraction β of v_o is feedback to (+) terminal, where $\beta = \frac{R_2}{R_1 + R_2}$. Here R_1 and R_2 act as voltage divider. v_o is also feedback through R to the (-) terminal. Whenever voltage v_c at (-) terminal exceeds V_{ref}, opamp changes its state, since it acts as a comparator.

Operation:

Let $v_o = + V_{Sat}$

$\therefore V_{ref} = \beta v_o = + \beta V_{Sat}$

Now capacitor C starts charging towards v_o though R. When voltage across capacitor just exceeds $+\beta v_o$, opamp o/p switches to $- V_{Sat}$ and the cycle repeats.

Derivation for time period 'T' of the o/p

We know that capacitor charge equation is given by

v_c (t) = v_f + $\left(v_i - v_f\right)e^{-t/RC}$ ….. (1)

where v_i = Initial voltage

v_f = Final (target) voltage

Consider 1st half cycle. i.e., v_o = + V_{Sat}

Here v_i = - βV_{Sat} and v_f = + V_{Sat}

∴ Eq. (1) becomes

v_c (t) = V_{Sat}+ $(-\beta V_{Sat} - V_{Sat})\, e^{-t/RC}$

= V_{Sat}– $V_{Sat}\,(1+\beta)\, e^{-t/RC}$ …… (2)

At t = T_1, v_c (t) = βV_{Sat}

∴ Eq. (2) becomes

$\beta V_{Sat} = V_{Sat} - V_{Sat}\,(1+\beta)\, e^{-T_1/RC}$

$= V_{Sat}\,\{1 - (1+\beta)\, e^{-T_1/RC}\}$

i.e., $\beta = 1 - (1+\beta)\, e^{-T_1/RC}$

i.e., $(1+\beta)\, e^{-T_1/RC} = 1 - \beta$

Or $e^{-T_1/RC} = \frac{1-\beta}{1+\beta}$

Or $e^{T_1/RC} = \frac{1+\beta}{1-\beta}$

Taking logarithms on both sides of above equation, we get

$$\frac{T_1}{RC} = \ln\left\{\frac{1+\beta}{1-\beta}\right\}$$

Or T_1 = RC. ln $\left\{\frac{1+\beta}{1-\beta}\right\}$

Total time period T = 2 T_1

i.e., T = 2 RC. ln $\left\{\frac{1+\beta}{1-\beta}\right\}$

and frequency of output = $\frac{1}{T}$

Problem 2.6: In the square wave oscillator of Fig. 7 (a), calculate the frequency of oscillations if R_2 = 10 KΩ, R_1 = 11.6 KΩ, R = 100 KΩ and C = 0.01 μF.

Solution:

We know that the time period of the square wave output is

$T = 2\,RC.\ln\left\{\frac{1+\beta}{1-\beta}\right\}$

Given that R_2 = 10 KΩ, R_1 = 11.6 KΩ, R = 100 KΩ;

C = 0.01 μF = 0.01 x 10^{-6} F = 10^{-8} F

$\beta = \frac{R_2}{R_1+R_2} = \frac{10\ K\Omega}{(10+11.6)\text{K}\Omega} = \frac{10}{21.6}$

$\frac{1+\beta}{1-\beta} = \frac{1+{}^{10}/_{21.6}}{1-{}^{10}/_{21.6}}$h

= 2.7241

∴ T = 2 x 100 x 1000 x 10^{-8} x ln (2.7241)

= 2.04 mSec

Frequency = $\frac{1}{T} = \frac{1}{2.04\ x\ 10^{-3}}$ = 0.4902 KHz

Problem 2.7: Design a square wave oscillator for f = 1 KHz. The opamp is a 741 with supply voltages ± 15 V.

Solution:

Consider Fig. 7 (a)

Let R1 = R2 = 10 KΩ

Then $\beta = \frac{R_2}{R_1+R_2} = \frac{1}{2}$

We know that the period of square wave o/p is

$T = 2\,RC.\ln\left\{\frac{1+\beta}{1-\beta}\right\}$

Chose C = 0.01μF = 10^{-8} F

Since f = 1000 Hz, T = $\frac{1}{1000}$ = 10^{-3} Sec

∴10^{-3} = 2 x R x 10^{-8}x ln $\left\{\frac{1+\frac{1}{2}}{1-\frac{1}{2}}\right\}$

= 2R x 10^{-8} x ln3

$\therefore$ R = $\frac{10^{-3}}{2\ x\ 10^{-8}\ x\ ln3}$

= 0.45512 x 10^{-5}

= 45.512 KΩ

To make o/p independent of supply voltage:

Amplitude of o/p depends on power supply voltage. To make the o/p independent of supply voltage, we use 2 back-to-back connected Zener diodes as shown in Fig. 7 (b). Fig. 7 (c) shows the waveform for v_o.

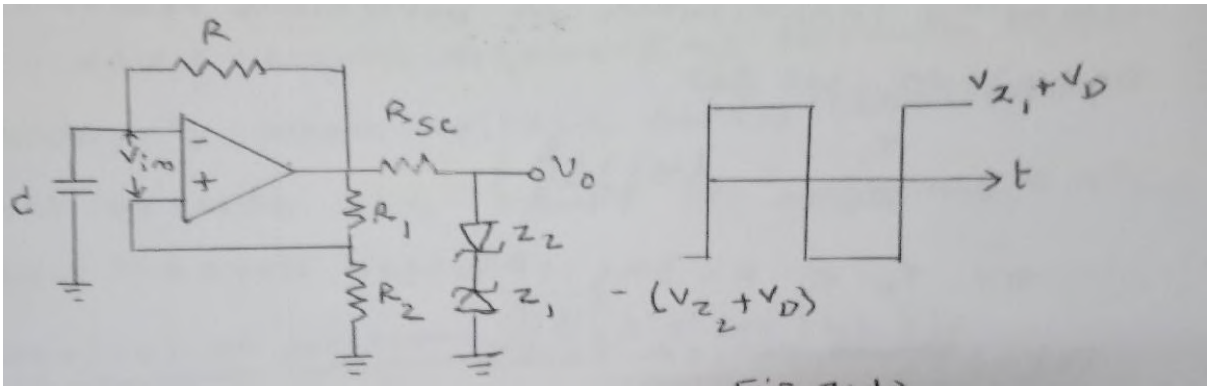


Fig. 7 (b) Zener diode Circuit **Fig. 7 (c) v_o waveform**

When v_o = + $V_{Sat,}$ diode Z_1 breaks down and Z_2 conducts.

$\therefore v_o = v_{Z_1} + v_D$

When v_o = - V_{Sat}

Z_1 is forward biased and Z_2 is reverse biased and operates in breakdown reion.

$$\therefore v_o = -(v_{Z_2} + v_D)$$

Where v_{Z_1} and v_{Z_2} are Zener breakdown voltages of Z_1 and Z_2. V_D is the forward bias voltage drop across each diode.

Resistor R_{sc} in Fig. 7 (b) is used to limit the currents drawn from opamp to

$$I_{sc} = \frac{V_{Sat} - VZ}{R_{sc}} \{\text{if } v_{Z_1} = v_{Z_2} = V_Z\}$$

The circuit works well at audio frequencies. At high frequencies, operation is limited by slew rate of opamp.

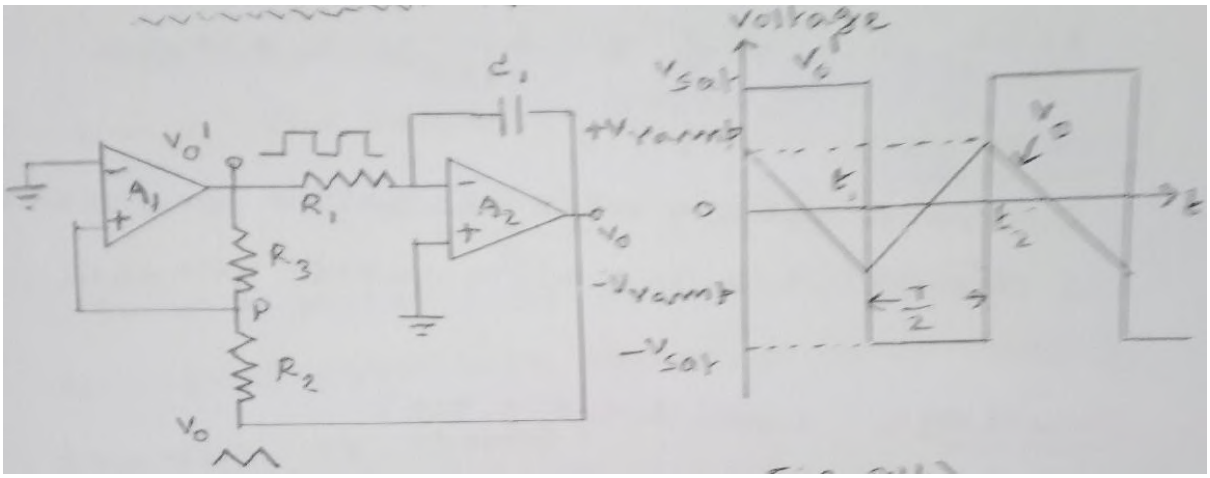
If two Zener diodes are identical, $v_{Z_1} = v_{Z_2} = V_Z$

Then we get a symmetrical square wave. Otherwise

($i.e., v_{Z_1} \neq v_{Z_2}$), we get an assymetric square wave o/p

TRIANGULAR WAVE GENERATOR

Fig. 8 (a) shows a triangular wave generator.Here A_1 generates a square wave with output v_o'. It is integrated by A_2 to get triangular wave with output v_o. Fig. 8 (b) shows the waveforms for v_o' and v_o.



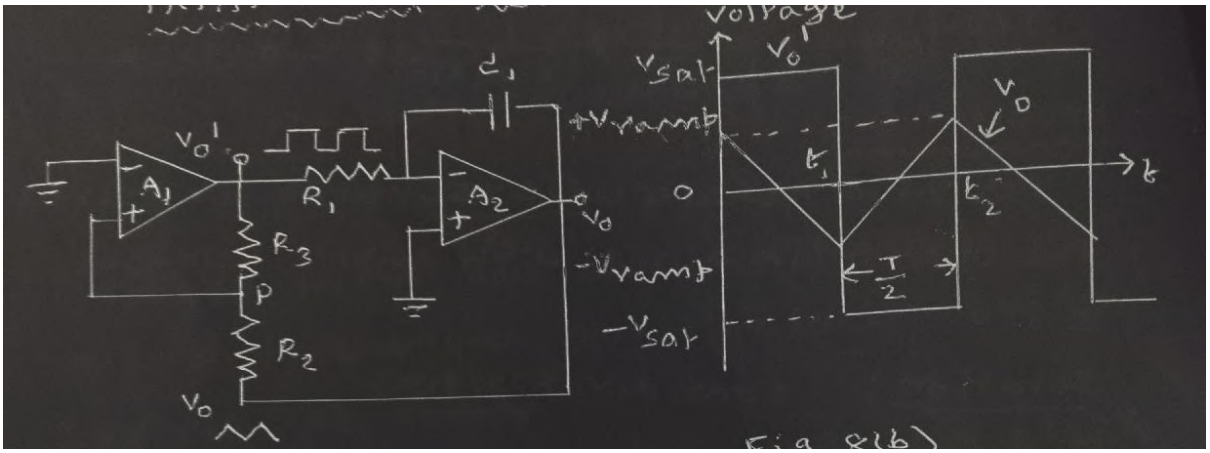


Fig. 8 (a) **Fig. 8 (b)**

v_o is again feedback to (-) input of A_1 through voltage divider R_2R_3.

Amplitude of v_o' = ± V_{Sat}

Operation of the circuit:

Let the initial o/p of comparator A_1 is + V_{Sat}. A_2 integrates this and gives a – ve going ramp as shown in fig. 8 (b). Thus, upper end of R_2R_3 is at an + V_{Sat} and lower end is at – ve going ramp. The voltage at point P(i.e., V_P) becomes <0 V, when – ve going ramp reaches a voltage – V_{ramp} (say). This switches o/p of A1 to - V_{Sat}. Theno/p of A_2 increases in + ve direction. Again, when voltage at P becomes just more than 0, o/p of A1 switches to + V_{Sat}. The cycle repeats and generates a triangular waveform.

Frequency of Δ^{lar} wave is same as that of square wave. But amplitude of Δ^{lar} wave depends on RC value of integrator A_2 and voltage level of A_1. The o/p of A_1 can be controlled by using appropriate Zener diodes.

Derivation for Time period/Frequency:

When $v_o{}' = + V_{Sat}$

$V_P = - V_{ramp} \cdot \frac{R_3}{R_2 + R_3} + V_{Sat} \cdot \frac{R_2}{R_2 + R_3}$ ..... (1)

At $t = t_1$, $V_P = 0$

∴ Eq. (1) becomes

$- V_{ramp} \cdot \frac{R_3}{R_2 + R_3} = - V_{Sat} \cdot \frac{R_2}{R_2 + R_3}$

i.e., $- V_{ramp} = - \frac{R_2}{R_3} V_{Sat}$ ..... (2)

Similarly, at t = t2, o/p of A1 switches from $- V_{Sat}$ to $+ V_{Sat}$ and o/p of A2 is $+ V_{ramp}$.

So eq. (1) $\Rightarrow V_{ramp} = - \frac{R_2}{R_3} (- V_{Sat}) = + \frac{R_2}{R_3} (V_{Sat})$ .... (3)

From eqs. (2) and (3), we get

peak to peak amplitude of Δ^{lar} wave

$v_{o(pp)} = + V_{ramp} - (- V_{ramp})$

$= 2 \frac{R_2}{R_3} V_{Sat}$ ..... (4)

Basic integrator equation is

$v_o = \frac{-1}{RC} \int v_i dt$ .... (5)

$v_o = v_{o(pp)}$, $R = R_1$, $C = C_1$

From Fig. 8 (b), we see that, for 2nd half cycle $\frac{T}{2}$, o/p switches from $- V_{ramp}$ to $+ V_{ramp}$,

$v_i = V_{Sat}$

i.e., eq. (5) $\Rightarrow$

$v_{o(pp)} = \frac{-1}{R_1 C_1} \int_0^{\frac{T}{2}} (- V_{Sat}) \, dt$

$= \frac{V_{Sat}}{R_1 C_1} \cdot \left(\frac{T}{2}\right)$

$2 \frac{R_2}{R_3} V_{Sat} = \frac{V_{Sat} \cdot T}{2 R_1 C_1}$ using eq. (4)

i.e., T = $\frac{4\,R_1R_2C_1}{R_3}$

∴ Frequency of Δ^{lar} wave = $f_o = \frac{1}{T} = \frac{R_3}{4\,R_1R_2C_1}$

Problem 2.8: For the circuit in Fig. 8 (a), R_1 = 10 KΩ, R_2 = 10 KΩ, C_1 = 0.1 μF, R_3 = 40 KΩ. Find the frequency of Δ^{lar} wave.

Solution:

Frequency of Δ^{lar} wave = $f_o = \frac{R_3}{4\,R_1R_2C_1}$

$$= \frac{40\ x\ 10^3}{4\ x\ 10\ x\ 1000\ x\ 10\ x\ 1000\ x\ 0.1\ x\ 10^{-6}}$$

= 1000 Hz = 1 KHz

MONOSTABLE MULTIVIBRATOR

It has one stable state and one quasi (semi) stable state. When a triggering pulse is given, it generates single o/p pulse. Width of this pulse depends on external components connected to opamp.

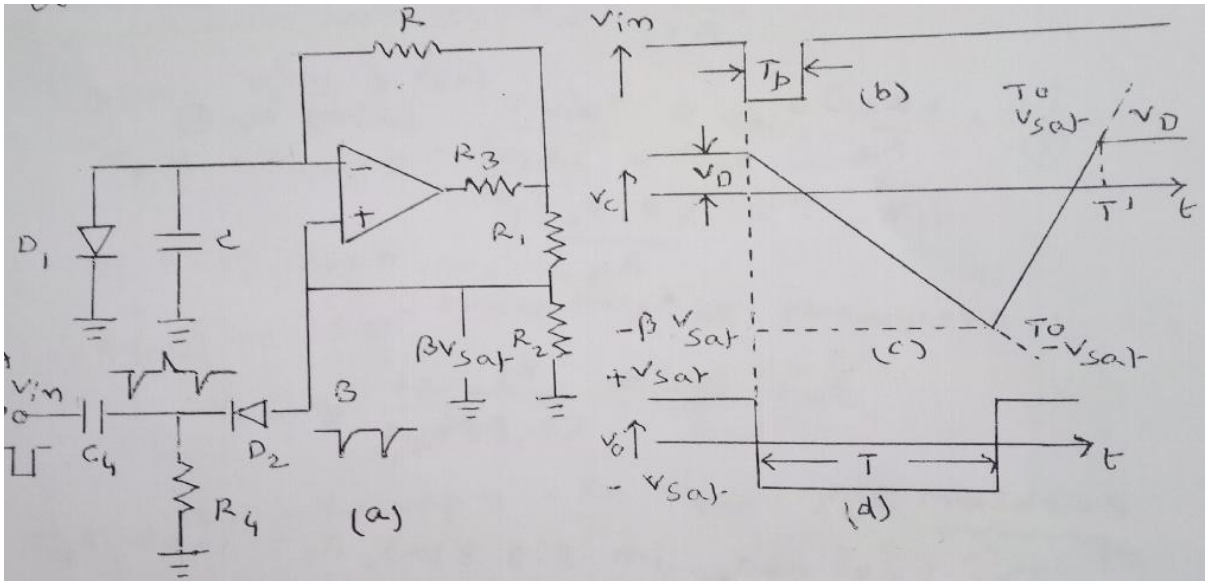


Fig. 9 (a)

Fig. 9 (a) represents a modified form of astable multivibrator. Diode D1 acts as a clamper. When o/p is + V_{Sat}, it clamps the capacitor voltage v_c to 0.7 V.

Consider points A and B.

A – ve going pulse is applied at A. It passes through differentiator R_4C_4 and diode D_2 (clipper) and gives a – ve going triggering pulse at point B. This pulse is applied to the (+) input terminal of opamp. Here v_o is o/p of circuit.

In steady state, let v_o = + V_{Sat}

So D_1 conducts and clamps v_c to 0.7 V.

The voltage at the (+) input terminal through voltage divider R_1R_2 is + β V_{Sat}.

Now, let a trigger of negative magnitude 'V_1' is applied to (+) input terminal, so that effective signal at this terminal is < 0.7 V

i.e., {βV_{Sat} + (- V1)}< 0.7 V

So, o/p of opamp will switch from + V_{Sat} to - V_{Sat}.

Now D_1 will be reverse biased. So, capacitor 'C' charges exponentially to - V_{Sat} through resistor R.

The voltage at (+) input terminal, now, is - β V_{Sat}

when v_c just crosses - β V_{Sat}, opamp o/p switches back to + V_{Sat}.

Then C starts charging to +V_{Sat} through R until v_c = 0.7 V. i.e., until v_c is clamped to 0.7 V.

Fig. 9 (b), 9 (c) and 9 (d) show various waveforms.

Derivation for pulse width 'T':

We know that capacitor charge equation is given by

v_c (t) = v_f + $\left(v_i - v_f\right)e^{-t/RC}$ ….. (1)

where v_i = Initial value

v_f = Final (target) value

For the circuit, $v_f = -V_{Sat}$

$v_i = V_D$ (diode forward voltage)

∴ Eq. (1) becomes

v_c (t) = $-V_{Sat}$ + $(V_D + V_{Sat})e^{-t/RC}$ …… (2)

But, at t = T_1, v_c = - β V_{Sat}

∴ Eq. (2) becomes

- β $\cancel{V_{Sat}}$ = - $\cancel{V_{Sat}}$ + $\cancel{V_{Sat}}\left(1 + \frac{V_D}{V_{Sat}}\right)e^{-T/RC}$

i.e., - β = - 1 + $\left(1 + \frac{V_D}{V_{Sat}}\right)e^{-T/RC}$

$\left(1 + \frac{V_D}{V_{Sat}}\right)e^{-T/RC} = 1 - \beta$

i.e., $e^{-T/RC} = \frac{1-\beta}{\left(1+\frac{V_D}{V_{Sat}}\right)}$

$e^{T/RC} = \frac{1+V_D/V_{Sat}}{1-\beta}$

Taking logarithms on both sides, we get

$T/RC = \ln\left\{\frac{1+V_D/V_{Sat}}{1-\beta}\right\}$

i.e., $\mathbf{T = RC \ln\left\{\frac{1+V_D/V_{Sat}}{1-\beta}\right\}}$

where $\beta = \frac{R_2}{R_1+R_2}$

If $V_{Sat} \gg V_D$ and $R_1 = R_2$

$\beta = \frac{1}{2} = 0.5$

$T = RC \ln \frac{1}{1-0.5} = RC \ln 2 = 0.69RC$

So approximate formula is **T= 0.69RC**

Recovery time:

v_c again reaches V_D at T', Where T' > T. Then (T' – T) is called '**recovery time'.**

A second triggering pulse can be given only after recovery time. Otherwise, operation is ambiguous.

Note1: For proper monostable operation

$$T_p \ll T$$

Where T_p and T are widths of triggering pulse and o/p respectively.

Note2: Monostable multivibrator is also called "Gating Circuit" or "One shot".

Problem 2.9: Design a monostable multivibrator with trigger pulse shaping which will drive a LED "ON" for 0.5 Second each time it is pulsed.

Solution:

Pulse width T of a monostable multivibrator is given by

$T = RC \ln \left\{ \frac{1+{}^{V_D}/_{V_{Sat}}}{1-\beta} \right\}$

where $\beta = \frac{R_2}{R_1+R_2}$

Given that T = 0.5 Sec

If $V_{Sat} \gg V_D$, $\quad 1 + {}^{V_D}/_{V_{Sat}} = 1$

Let $R_1 = R_2$

$\therefore \beta = \frac{R_2}{R_1+R_2} = \frac{1}{2} = 0.5$

$T = RC \ln \frac{1}{1-0.5} = RC \ln 2 = 0.69RC$

Choose R = 100 KΩ

Then $C = \frac{T}{0.69\ R}$

$= \frac{0.5}{0.69\ x\ 100\ x\ 10^3} =$

Sample and Hold Circuit

A Sample and Hold circuit samples an i/p signal and holds on to its last sampled value until i/p is sampled again.

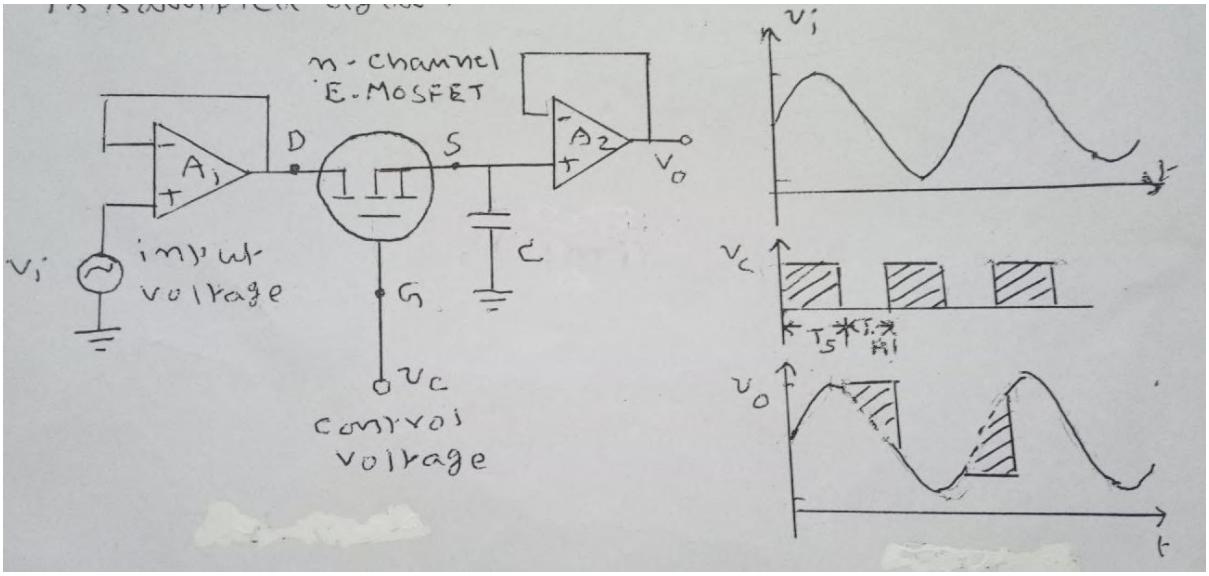


Fig. 10 (a) Sample and Hole circuit

Fig. 10 (b) Waveforms

Fig. 10 (a) represents a sample and hold circuit. n-channel E-MOSFET acts as a switch. It is controlled by control voltage v_c. v_i is the analog i/p voltage to be sampled. v_i is applied to the Drain (D) of MOSFET and v_c is applied to the Gate (G) of MOSFET. Capacitor 'C' stores the charge.

When v_c = + ve:

The MOSFET is ON and C charges to the instantaneous value of v_i with a time constant $=(R_o + r_{DS(ON)})C$

where R_o is the o/p resistance of A_1 and $r_{DS(ON)}$ is the ON resistance of MOSFET.

Thus, i/p voltage v_i appears across C and then at the o/p of voltage follower A_2

When v_c = 0:

MOSFET is OFF. C now faces the high i/p impedance of voltage follower A_2. So, it can't discharge. C holds the voltage across it. Fig. 10 (b) shows various waveforms.

Sample Period T_S: It is the time during which voltage across C becomes v_i.

Hold Period T_H: Time during which voltage across C is held constant.

Note: Control voltage frequency ≥ 2 * input frequency

Applications of Sample and Hold Circuit:

- Digital interfacing,
- ADC systems
- Pulse Code Modulation (PCM) Systems

ANALOG MULTIPLIER

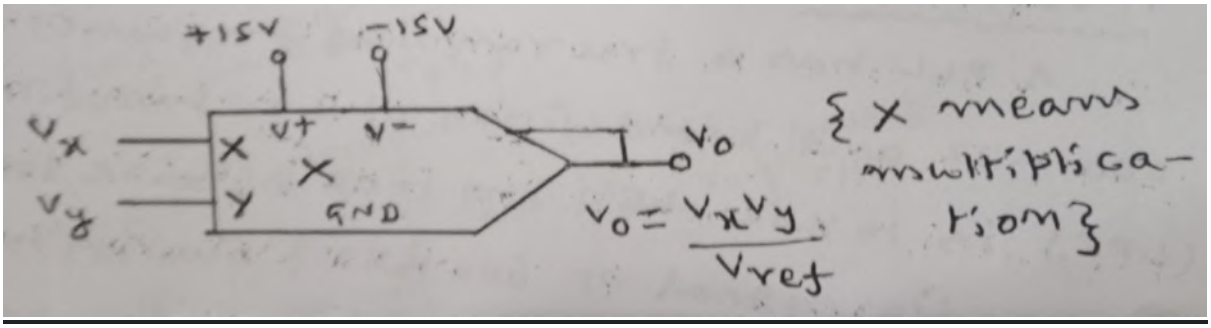


Fig. 11: Analog Multiplier

Fig. 11 shows the symbol of analog multiplier with 2 input signals v_x and v_y. Output is the product of these two inputs divided by reference voltage V_{ref}. Thus, the o/p is the scaled version of x and y inputs. The o/p voltage is given by

$$\mathbf{vo} = \frac{v_x v_y}{V_{ref}}$$

Normally V_{ref} is set to 10 mV.

So, $v_o = \frac{v_x v_y}{10}$

As long as

$$v_x < V_{ref} \text{ and } v_y < Vref,$$

the output of the multiplier will not saturate. Power supply voltage can range from ± 8V to ± 18V. For 741 opamp it is ± 15 V.Squaring a signal

Quadrants of operation: If both inputs re + ve, the IC is said to be a **one quadrant multiplier**. If one input is held positive and other input is allowed to swing either + ve or – ve, it is called **two quadrant operation**. If both inputs are allowed to swing either + ve and – ve, the IC is called a **fourquadrant multiplier**.

Applications of Analog Multiplier:

i. Frequency doubling
ii. Measurement of real power
iii. Detecting phase angle between 2 signals
iv. Multiplying 2 analog signals
v. Dividing one signal by other
vi. Finding square root of a signal
vii. Squaring a signal

ANALOG DIVIDER

Fig. 12 shows an analog divider circuit.

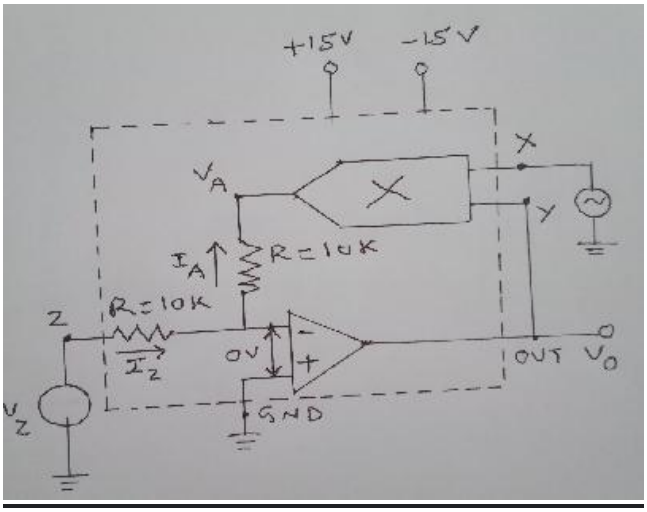


Fig. 12: Multiplier IC configured as analog divider

Here, the multiplier element is placed in opamp's feedback loop.

Let v_x and v_y be the input signals.

Then $v_o = - V_{ref}\frac{v_x}{v_y}$

Derivation of above result:

For ideal opamp, no current flows through (+) terminal.

So, From figure, $I_z = I_A$ …. (1)

Also, $I_z = \frac{v_z - 0}{R}$

$= \frac{v_z}{R}$ ….. (2)

The o/p voltage of multiplier is given by

$V_A = \frac{v_x v_y}{V_{ref}} = \frac{v_x v_o}{V_{ref}}$ (Since $v_y = v_o$) … (3)

But $I_A = \frac{0 - V_A}{R}$

$= \frac{-V_A}{R}$

$= - \frac{v_x v_o}{v_{ref} R}$ …. (4) using eq. (3)

From figure, $V_z = I_z R$ from eq. (2)

$= I_A R$ from eq. (1)

$= - \frac{v_x v_o}{v_{ref}}$ (using eq. (4))

i.e., $\boldsymbol{v_o = - V_{ref}\frac{v_z}{v_x}}$

Note: division by 0 is prohibited. i.e., v_x can't be zero.

Application: Multiplier IC is used for squaring a signal and divider circuit is used for finding square root of the signal.

LOGARITHMIC AMPLIFIER

Logarithmic Amplifier (log-amp) is defined as an amplifier circuit whose o/p is directly proportional to the logarithm of the i/p.

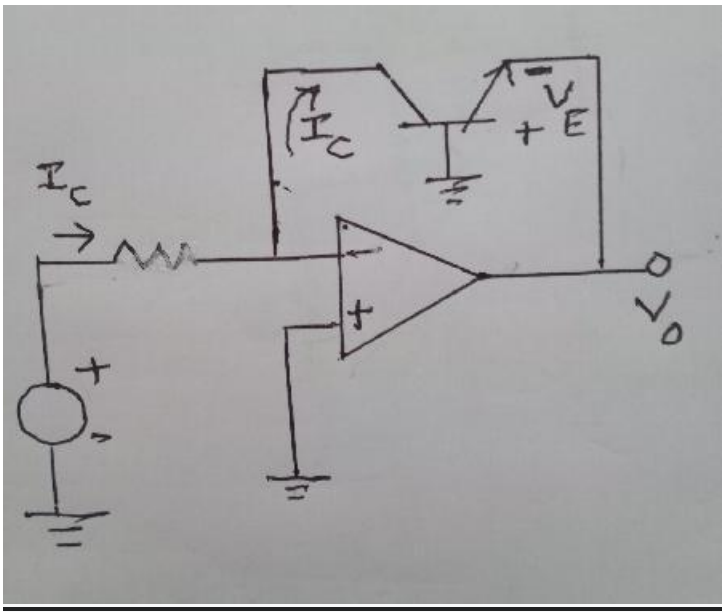


Fig. 13 (a) : Log amplifier

Fig 13. (a) shows a fundamental log-amp circuit, where a grounded base transistor is placed in the feedback path of an opamp.

Let us assume an ideal opamp. i.e., there exists a virtual ground at the input of opamp. So, collector is placed at virtual ground. Since base is also grounded, the transistor acts similar to a diode.

i.e., $I_E = I_s \left(e^{qV_e/kT}\right)$

For a grounded base transistor, $I_C = I_E$

i.e., $I_C = I_s \left(e^{qV_E/kT}\right)$

where I_s = emitter saturation current = Reverse saturation current of diode = 10^{-13} A

k = Botzmann's constant

T = Absolute temperature (in ^{0} K)

$\therefore \frac{I_C}{I_s} = \left(e^{qV_E/kT}\right)$

Or $e^{qV_e/kT} = \frac{I_C}{I_s} + 1 \approx \frac{I_C}{I_s}$ (Since $I_s \approx 10^{-13}$ A, $I_C > I_s$)

Taking natural logarithms on both sides, we get

$qV_E/_{kT} = \ln\left(\frac{I_C}{I_s}\right)$

Or $V_E = \frac{kT}{q}\ln\left(\frac{I_C}{I_s}\right)$ …. (1)

From Fig.

$I_C = \frac{V_i}{R_1}$ and $V_E = -V_o$

Substituting the values of I_C and V_E in eq. (1), we get

$$V_o = -\frac{kT}{q}\ln\left(\frac{V_i}{R_1 I_s}\right)$$

$$= -\frac{kT}{q}\ln\left(\frac{V_i}{V_{ref}}\right)$$

where $V_{ref} = R1Is$

Thus, the o/p voltage is directly proportional to the logarithm of i/p voltage

Note: $\log_{10} X = 0.4343 \ln X$

This circuit has a problem. The emitter saturation current $I_s$varies from transistor to transistor. It also depends on temperature. Hence stable reference voltage V_{ref} cannot be obtained.

This problem can be avoided by using the modified circuit shown in Fig.

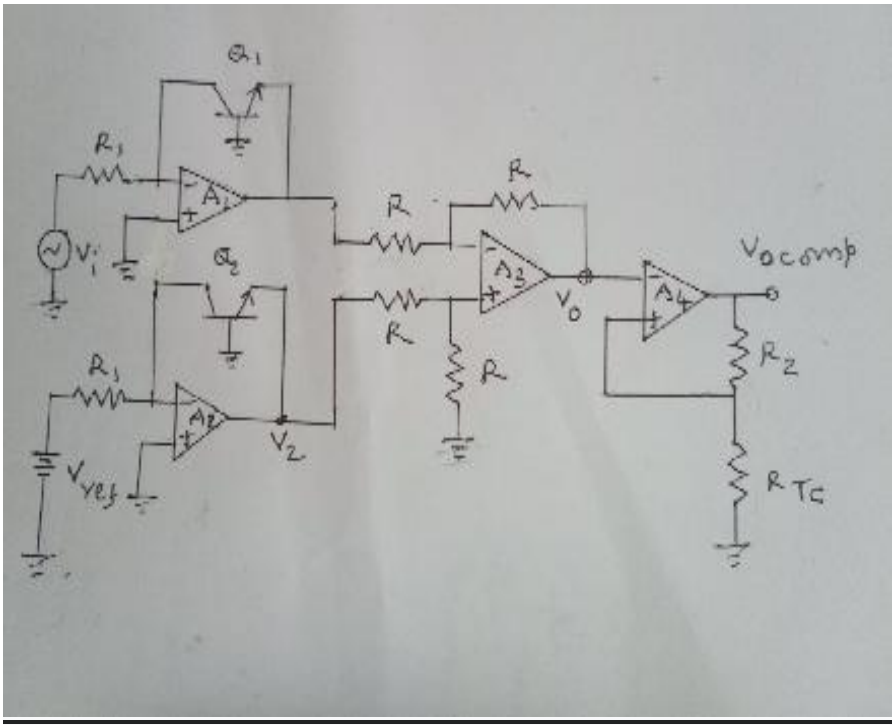


Fig. 13 (b): Modified log-amp

Here the i/p is applied to one log-amp while reference voltage is applied to another log-amp. The 2 transistors are integrated close together in the same silicon wafer. This provides a close march of saturation currents and ensures good thermal tracking.

Let Is1 = Is2 = Is

Then

$V_1 = -\frac{kT}{q}\ln\left(\frac{V_i}{R_1 I_s}\right)$ and

$V_2 = -\frac{kT}{q}\ln\left(\frac{V_{ref}}{R_1 I_s}\right)$

So, $V_o = V_2 - V_1$

$=\frac{kT}{q}\left[\ln\left(\frac{V_i}{R_1 I_s}\right) - \ln\left(\frac{V_{ref}}{R_1 I_s}\right)\right]$

$= \frac{kT}{q}\ln\left[\left(\frac{V_i}{R_1 I_s}\right) / \left(\frac{V_{ref}}{R_1 I_s}\right)\right]$

$= \frac{kT}{q}\ln\left[\frac{V_i}{R_1 I_s}.\frac{R_1 I_s}{V_{ref}}\right]$

$= \frac{kT}{q}\ln\left[\frac{V_i}{V_{ref}}\right]$

Thus, reference voltage is now set with a single external voltage source. Its dependence on device and temperature was removed. The voltage V_o is still dependent on temperature and is directly proportional to T. This is compensated by the last opamp stage A_4 which provides a non-inverting gain of

$\left(1 + \frac{R_2}{R_{TC}}\right)$.

Now Vo comp = $\left(1 + \frac{R_2}{R_{TC}}\right).\frac{kT}{q}\ln\left[\frac{V_i}{V_{ref}}\right]$

where R_{TC} is a temperature sensitive resistance with a positive coefficient of temperature (sensistor) so that slope of equation becomes constant as temperature changes.

ANTILOG AMPLIFIER

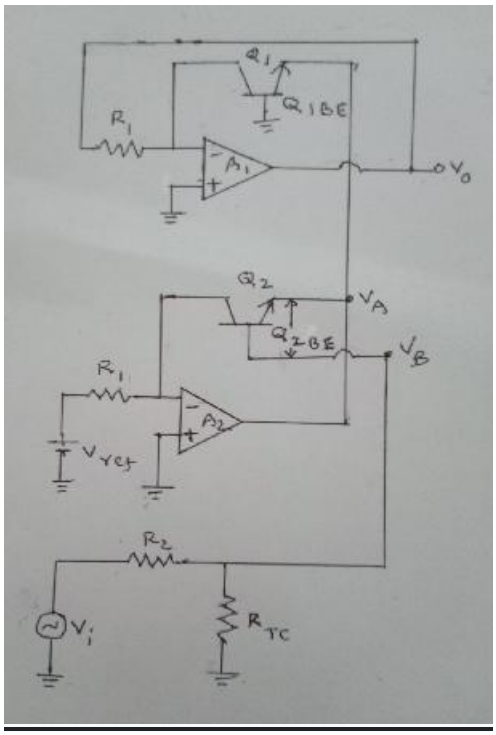


Fig. 14: Antilog Amplifier

Fig. 14 shows an antilog amplifier. The input V_i is applied to the base of transistor Q_2 through the voltage divider R_2 and R_{TC}. The output V_o is feedback to the (-) input of A_1 through the resistor R_1. The base to emitter voltage of transistors $_{Q1}$ and Q_2 can be written as

$$V_{Q1\,B-E} = \frac{kT}{q}\ln\left(\frac{V_o}{R_1 I_s}\right) \quad ,,,,,, \quad (1)$$

and $$V_{Q2\,B-E} = \frac{kT}{q}\ln\left(\frac{V_{ref}}{R_1 I_s}\right) \quad \ldots\ldots \quad (2)$$

Since the base of Q_1 is tied to ground, we get

$$V_A = -\,V_{Q1\,B-E} = -\,\frac{kT}{q}\ln\left(\frac{V_o}{R_1 I_s}\right) \quad \ldots.. \quad (3)$$

the base voltage V_B of Q_2 is

$$V_B = \left\{\frac{R_{TC}}{R_2 + R_{TC}}\right\} V_i \quad \ldots.. \quad (4)$$

The voltage at the emitter of Q_2 is

$$V_{Q2\,B-E} = V_B + V_{Q2\,E-B}$$

$$= \left\{\frac{R_{TC}}{R_2 + R_{TC}}\right\} V_i - \frac{kT}{q}\ln\left(\frac{V_{ref}}{R_1 I_s}\right) \ldots\ldots \quad (5) \qquad \{\text{using eqs. (2) and (4)}\}$$

But emitter voltage of Q_2 is V_A.

i.e., $V_A = V_{Q2\ B-E}$ ..... (6)

Or $-\frac{kT}{q}\ln\left(\frac{V_o}{R_1 I_s}\right) = \left\{\frac{R_{TC}}{R_2 + R_{TC}}\right\}V_i - \frac{kT}{q}\ln\left(\frac{V_{ref}}{R_1 I_s}\right)$

Or $\left\{\frac{R_{TC}}{R_2 + R_{TC}}\right\} Vi = -\frac{kT}{q}\left[\ln\left(\frac{V_o}{R_1 I_s}\right) - \ln\left(\frac{V_{ref}}{R_1 I_s}\right)\right]$

Or

$\frac{q}{kT}.\left\{\frac{R_{TC}}{R_2 + R_{TC}}\right\} Vi = \ln\left(\frac{V_o}{V_{ref}}\right)$

Question Bank on Unit-2.

1. Draw the circuit diagram of a non-inverting/Inverting amplifier.Explain its operation. Derive an expression for its closed loop voltage gain.
2. Describe the operation of a voltage follower.
3. Describe an inverting adder with three inputs and derive an expression for its output.
4. Describe the operation of V to I and I to V converters.
5. With the help of a neat diagram explain the operation of an instrumentation amplifier and derive necessary expression for its output.
6. Draw and explain the operation of a practical Differentiator/Integrator. Describe its frequency response characteristics
7. With the help of a neat circuit diagram and waveforms, explain the operation of an inverting/non-inverting comparator.
8. With the help of a neat circuit diagram and waveforms, explain the operation of an astable multivibrator (Square wave generator).
9. With the help of a neat circuit diagram and waveforms, explain the operation of a monostable multivibrator.
10. With the help of a neat circuit diagram and waveforms, explain the operation of a triangular wave form generator.
11. With the help of a neat circuit diagram and waveforms, explain the operation of a Schmitt Trigger circuit.
12. Explain an (a) Analog multiplier (b) Analog divider.
13. With the help of a neat circuit diagram and waveforms, explain the operation of a sample and hold circuit.

2 Marks Questions

1. What are the applications of V-I and I-V converters??
2. Describe a voltage follower.
3. Mention the applications of analog multiplier.
4. What are the 4 quadrants of an analog multiplier?
5. What are the applications of comparators?
6. What are the applications of zero-crossing detector?
7. Why back-to-back connected Zener diodes are used in the output of a square wave generator?
8. What is recovery time in a monostable multivibrator? What is its significance?
9. Define 'Sample period and 'hold period in case of a sampling and hold ciruit.
10. What are the applications of Sample and Hold Circuit?
11. Draw the frequency response of ideal and practical integrator.
12. What are the problems with a simple differentiator?
13. What are the problems with a simple integrator?
14. What are the applications of V-I converter?
15. Why compensating resistor is used?

Objective Questions

1. Expression of gain for the gain of an inverting amplifier is ----------
   (a) - $\frac{R_f}{R_i}$ (b) $1 + \frac{R_f}{R_i}$ (a) $\frac{R_f}{R_i}$ (b) $-(1 + \frac{R_f}{R_i})$
2. Expression of gain for the gain of a non-inverting amplifier is ----------
   (a) - $\frac{R_f}{R_i}$ **(b)** $\mathbf{1 + \frac{R_f}{R_i}}$ (a) $\frac{R_f}{R_i}$ (b) $-(1 + \frac{R_f}{R_i})$
3. Floating load means
   (a) Load impedance is shorted (b) Load impedance is open circuited (c) One end of it is grounded **(iv) No end is grounded**.
4. --------- is used in low voltage ac and dc voltmeters.
   (a) V-I converter(b) I-V converter (c) Any one (d) none
5. ---------- has problems at high frequencies.
   (a) Differentiator(b) Integrator (c) Both (d) None
6. ---------- has problems at low frequencies.
   (a) Differentiator **(b) Integrator** (c) Both (d) None
7. For an ideal differentiator, when $f > f_b$, gain changes at a rate of ------
   (a) + 20 dB per decade (b) -20 dB per decade (c) Gain is constant (d) none
8. For an inverting amplifier, the phase angle between input and output is
   (a) 0^0(b) 90^0**(c)** $\mathbf{180^0}$(d) None

9. For a non-inverting amplifier, the phase angle between input and output is
   (a) 0^0(b) 90^0 (c) 180^0(d) None
10. Which passive component blocks dc component
   (a) R (b) L **(c) C** (d) None
11. What is the application of a comparator?
   (a) Zero-crossing detector (b) Phase meters (c) Schmitt Trigger **(d) All**
12. A free running oscillator means --------
   (a) An astable multivibrator (b) A monostable multivibrator (c) A Schmitt Trigger (d) A Triangular wave generator
13. Which device is used in sample and hold circuit?
   (a) Diode (b) Transistor (c) FET **(d) MOSFET**
14. Which device is used for squaring a given signal?
   (a) Analog divider **(b) Analog multiplier** (c) Differentiator (d) Integrator
15. What is the output of an integrator for a square wave input?
   (a) Series of pulses (b) Sinewave (c) Square wave **(d) Triangular wave**
16. If f = 10 f_a, accuracy of an integrator is ------- is
   (a) 99% (b) 100% (c) 0% (d) 50%
17. In Sample and hold circuit, the time during which voltage across C becomes $v_i$is called ----------
   (a)Hold period **(b)Sample Period**(c) Time period (d) None
18. Sample and hold circuit is used in
   (a) Digital interfacing (b) ADC Systems (c) PCM systems **(d) All**
19. Which of the following is correct?
   (a) An analog multiplier is used to realize an analog divider (b) An analog divider is used to realize an analog multiplier (c) Both are correct (d) None of (a) and (b) are correct
20. The voltages to be added in aninverting summer are applied to the ----- terminal of OP-AMP.
   (a) Supply(b) Non-inverting (c) **Inverting**(d) None

Note: III UNIT Notes given in class

Question Bank on Unit-3

(Active Filters)

Big Questions

1. Derive an expression for the Transfer function of First order LPF/HPF
2. Derive an expression for the Transfer function of Second order LPF/HPF
3. Problem on the design of LPF and HPF.

4. What are active filters and passive filters? What are the advantages of active filters over passive filters?
5. (a) What is a band pass filter (BPF)? Derive an expression for Transfer Function of a wideband BPF.
   (b) Problem
6. What is the necessity of all pass filter? Draw its circuit diagram and derive an expression for its $\frac{v_o}{v_i}$. Comment on the phase shift generated by all pass filter.

2 Marks Questions

1. What are the advantages of active filters over passive filters?
2. What is the difference between BPF and BRF?
3. Draw the frequency response of first order LPF/HPF/BPF/BRF
4. Draw the frequency response of Second order LPF/HPF.
5. What is the application of all pass filters?
6. Write the expression of magnitude of Transfer function of First order LPF/HPF
7. What is the difference between wide and narrow BPF?
8. What is the difference between wide and narrow BPF?
9. Write the expression of magnitude of Transfer function of Second order LPF/HPF.
10. Write the expressions for f_o, Bandwidth and Q factor for a BPF.

Objective Questions

21. Active filters used in phase correction in analog systems are ------ filters.
    (a) Low pass (b) High pass (c) Band pass **(d) All pass**
22. The roll off rate for 2nd order HPF is
    (a) - 30 dB / decade**(b) - 40 dB / decade** (c) - 20 dB / decade(d) - 10 dB / decade
23. The roll off rate for 2nd order LPF is
    (a) - 30 dB / decade(b) - 40 dB / decade (c) - 20 dB / decade(d) - 10 dB / decade
24. The magnitude of transfer function of fist order LPF is**Ans: (b)**
    (a) $\frac{A_o}{\sqrt{1+\left(\frac{f_l}{f}\right)^2}}$ **(b)** $\frac{\boldsymbol{A_o}}{\sqrt{\mathbf{1}+\left(\frac{\boldsymbol{f}}{\boldsymbol{f_h}}\right)^{\mathbf{2}}}}$ (c) $\frac{A_o}{\sqrt{1+\left(\frac{f_l}{f}\right)^4}}$ (d) $\frac{A_o}{\sqrt{1+\left(\frac{f}{f_h}\right)^4}}$
25. The magnitude of transfer function of fist order HPF is**Ans:(a)**
    (a) $\frac{\boldsymbol{A_o}}{\sqrt{\mathbf{1}+\left(\frac{\boldsymbol{f_l}}{\boldsymbol{f}}\right)^{\mathbf{2}}}}$ (b) $\frac{A_o}{\sqrt{1+\left(\frac{f}{f_h}\right)^2}}$ (c) $\frac{A_o}{\sqrt{1+\left(\frac{f_l}{f}\right)^4}}$ (d) $\frac{A_o}{\sqrt{1+\left(\frac{f}{f_h}\right)^4}}$
26. The magnitude of transfer function of Second order LPF is**Ans:(d)**
    (a) $\frac{A_o}{\sqrt{1+\left(\frac{f_l}{f}\right)^2}}$ (b) $\frac{A_o}{\sqrt{1+\left(\frac{f}{f_h}\right)^2}}$ (c) $\frac{A_o}{\sqrt{1+\left(\frac{f_l}{f}\right)^4}}$ **(d)** $\frac{\boldsymbol{A_o}}{\sqrt{\mathbf{1}+\left(\frac{\boldsymbol{f}}{\boldsymbol{f_h}}\right)^{\mathbf{4}}}}$
27. The magnitude of transfer function of second order HPF is**Ans:(c)**
    (a) $\frac{A_o}{\sqrt{1+\left(\frac{f_l}{f}\right)^2}}$ (b) $\frac{A_o}{\sqrt{1+\left(\frac{f}{f_h}\right)^2}}$ **(c)** $\frac{\boldsymbol{A_o}}{\sqrt{\mathbf{1}+\left(\frac{\boldsymbol{f_l}}{\boldsymbol{f}}\right)^{\mathbf{4}}}}$ (d) $\frac{A_o}{\sqrt{1+\left(\frac{f}{f_h}\right)^4}}$

28. The damping factor of a Butterworth filter is
    (a) 1.06 (b) 1.73 **(c) 1.44**(d) .707
29. First order BPF is a cascade of first order------- followed by first order ------ respectively.
    (a) HPF, LPF (b) LPF, LPF (c) HPF, HPF (d) LPF, HPF
30. Expression for the f_o of BPF is --------
    (a) $f_h + f_l$ (b) $f_h f_l$ **(c)** $\sqrt{f_h f_l}$ (d) $f_h - f_l$

UNIT-3

ACTIVE FILTERS

Electrical Filter:

An Electrical Filter is a circuit that passes signals of specified frequencies and attenuates (rejects) signals of frequencies outside this band. Based on processing techniques, electrical filters are classified as analog filters and digital filters. Based on the type of elements used analog filters are classified as passive and active filters.

Passive Filters: (RC filters and LC filters)

They use passive components (R, L and C). LC filters (also called crystal filters) have high quality factor 'Q'. So, thy produce stable operation at high frequencies.

LC filters are not preferred at audio and low frequencies. It is because

- Inductors are bulky (large in size and heavy)
- They are costly.
- Stray magnetic fields are present due to magnetic coupling.

Thus, **RC filters** are used at audio and low frequencies.

Active Filters: They use opamps, resistors and capacitors. Here opamps are active components and R & C are passive components.

Advantages of active filters over passive filters:

- Opamps provide large gain. So, i/p signal is not attenuated as in passive filters.
- Opamps provide high i/p impedance and low o/p impedance. So, they do not cause loading of source and load.
- Because of high i/p impedance, we can use large resistor values. This reduces the need to use large capacitor values. (Large capacitors are bulky and costly).
- Opamps are less expensive and inductors are absent in active filters. So, they are more economical than passive filters.
- Active filters are easier to tune and adjust.

Disadvantages of active filters over passive filters:

- ✓ Opamps need two power supplies
- ✓ High frequency response of active filters is limited by the slew rate of the opamp.
- ✓ High frequency opamps are costly.
- ✓ There is a problem of oscillations in multi stage amplifiers.
- ✓ Since active filters use active devices, they are more susceptible to RF interference.
- ✓ In band pass filters and notch filters, practical considerations limit the value of Q factor to 50.

Types of Active Filters:

1. Low Pass Filters (LPFs):

They allow low frequency signals and attenuate high frequency signals > a cutoff frequency of f_h.

2. High Pass Filters (HPFs):

They allow high frequency signals and attenuate low frequency signals < a cutoff frequency of f_l.

3. Band Pass Filters (BPFs):

They allow a specified range of frequencies and reject frequencies outside this range.

4. Band Reject Filters (BRFs):

They attenuate a particular range of frequencies and allow frequency components outside this range.

Frequency Response of Active Filters:

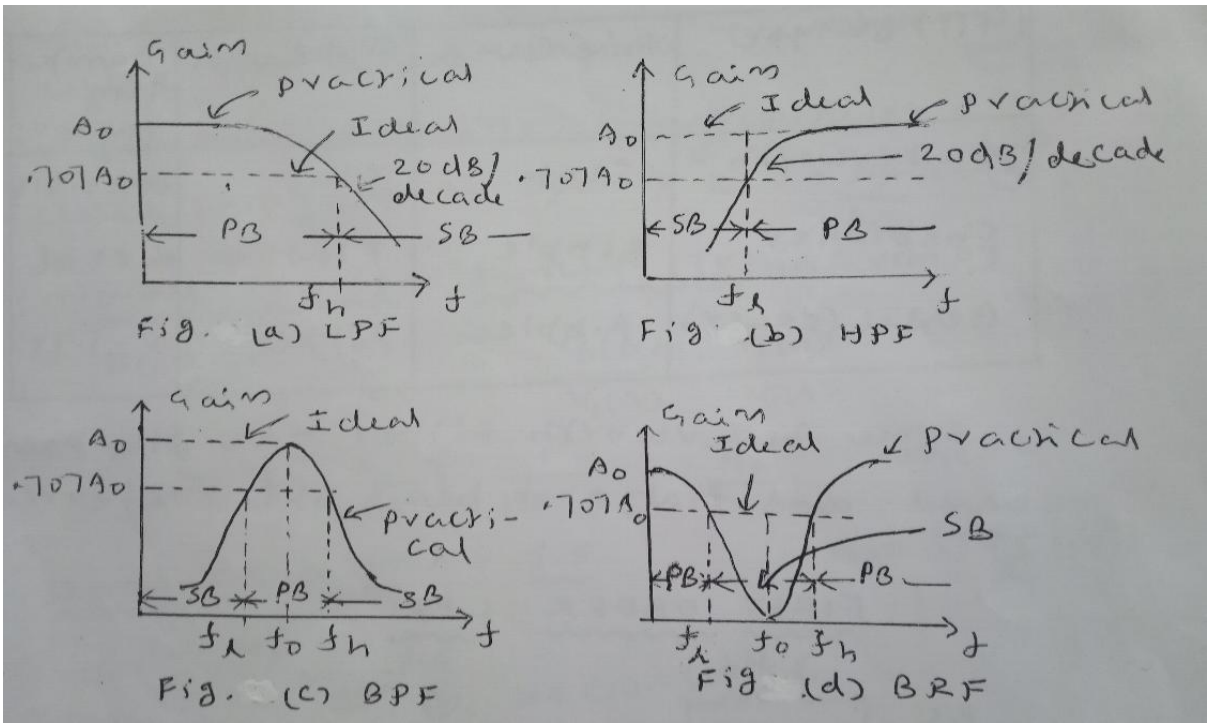


Fig. 1: Frequency Response of Active Filters

Fig. 1 represents the frequency response of the 4 types of active filters. Here frequency (in Hz) is taken on X-axis and gain is taken on Y-axis. Log scale is used for X-axis and linear scale is used for Y-axis.

Based on the design of filters, analog active filters are classified as Butterworth filters, Chebyshev filters and Bessel (Cauer) filters. This classification depends on the Transfer function.

Comparison of filters:

Filter Type	Pass Band	Stop Band	Damping factor
Butterworth	Flat	Flat	$\alpha = 1.44$
Chebyshev	Ripple	Flat	$\alpha = 1.06$
Bessel	Ripple	Ripple	$\alpha = 1.73$

Since Butterworth filter has flat pass band and flat stop band, it is preferred much.

First Order LPF

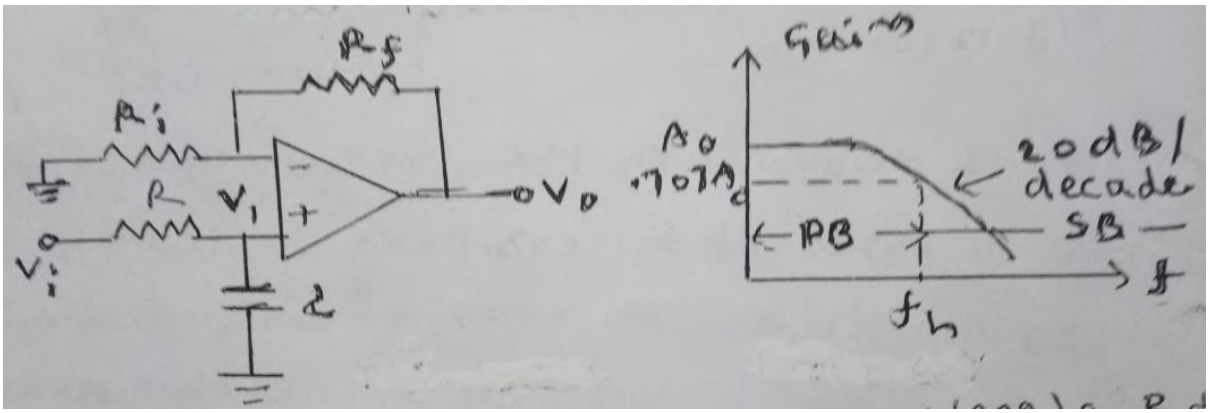


Fig. 2 (a): First Order LPF **Fig. 2(b) Frequency response**

A First Order LPF has a single RC network connected to the non-inverting terminal of opamp as shown in Fig. 2(a). Here v_i is the input voltage and v_o is the output.

Here R_i and R_f determine the gain of the filter.

Let v_1 be the voltage at the (+) input terminal of opamp.

$$\therefore v_1(s) = v_i(s).\frac{\frac{1}{sC}}{R+\frac{1}{sC}} = v_i(s).\frac{1}{1+sRC}$$

i.e., $\frac{v_1(s)}{v_i(s)} = \frac{1}{1+sRC}$ ……. (1)

where v (s) is the Laplace Transform of 'v' in time domain.

Closed loop gain of opamp = $\frac{v_o(s)}{v_1(s)} = 1 + \frac{R_f}{R_i}$ …….. (2)

Overall Transfer Function is given by

$$H(s) = \frac{v_o(s)}{v_i(s)} = \frac{v_o(s)}{v_1(s)} \cdot \frac{v_1(s)}{v_i(s)}$$

$$= \left(1 + \frac{R_f}{R_i}\right)\frac{1}{1+sRC} \quad \{\text{using eqs. (1) and (2)}\}$$

$$= \frac{A_o}{1+sRC} \quad \text{Where } A_o = 1 + \frac{R_f}{R_i} \quad \text{……. (3)}$$

Standard form of Transfer Function:

Let $\omega_h = \frac{1}{RC}$

Then from eq. (3), we can write

$$H(s) = \frac{A_o}{1+sRC} = \frac{A_o}{1+\frac{s}{\omega_h}} = \frac{A_o\omega_h}{s+\omega_h} \quad \text{……. (4)}$$

Frequency Response:

To determine the frequency response put s = jω in eq. (3). Then we get

$$H(j\omega) = \frac{A_o}{1 + j\omega RC}$$

$$= \frac{A_o}{1 + j2\pi fRC}$$

$$= \frac{A_o}{1 + {jf}/{(1/2\pi RC)}}$$

$$= \frac{A_o}{1 + {j\,f}/{f_h}} \quad \ldots\ldots \quad (5)$$

Where $f_h = \frac{1}{2\pi RC}$ or $\omega_h = \frac{1}{RC}$

Consider eq. (5).

When $f \ll f_h$, $|H(j\omega)| = \frac{A_o}{1+0} = A_o$

When $f = f_h$, $|H(j\omega)| = \frac{A_o}{\sqrt{1^2+1^2}} = \frac{A_o}{\sqrt{2}}$

When $f \gg f_h$, $|H(j\omega)| = \frac{A_o}{1+\infty} = 0$

Fig. 2 (b) shows the frequency response of first order LPF.

Important observations in Fig. 2(b):

i. Maximum gain is A_o at f = 0 Hz.
ii. At f_h, gain falls by ,707A_o (or – 3 dB below A_o when A_o is expressed in dB).
iii. Frequency response from 0 to f_h is called pass band.
iv. When f >f_h, gain decreases at a rate of 20 dB/decade.
v. Range of frequencies where f >f_h is called stop band

FIRST ORDER HPF

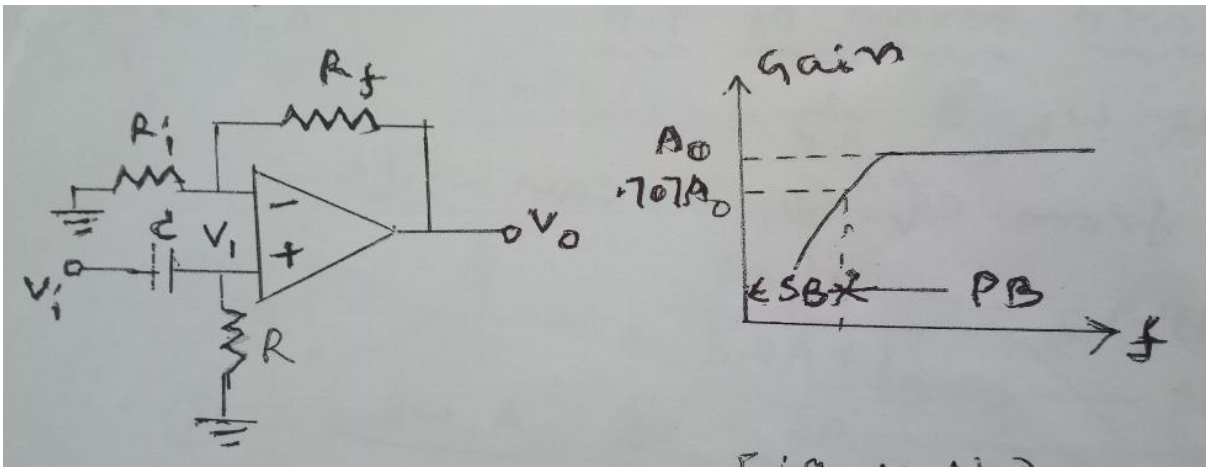


Fig. 3 (a): First Order HPF **Fig. 3 (b) Frequency response**

A first order HPF has a single RC network connected to the non-inverting terminal of opamp as shown in Fig. 3 (a). Note that, by interchanging the positions of R and C of a first order LPF, we will get a first order HPF.

Let the minimum frequency allowed by this filter is f_l.

Here R_i and R_f determine the gain of the filter.

Let $v_1$be the voltage at the (+) input terminal of opamp.

$\therefore v_1(s) = v_i(s).\frac{R}{R+\frac{1}{sC}} = v_i(s).\frac{sRC}{1+sRC}$

i.e., $\frac{v_1(s)}{v_i(s)} = \frac{sRC}{1+sRC}$ ..... (1)

where v (s) is the Laplace Transform of 'v' in time domain.

Closed loop gain of opamp = $\frac{v_o(s)}{v_1(s)} = 1 + \frac{R_f}{R_i}$ ..... (2)

Overall Transfer Function is given by

$H(s) = \frac{v_o(s)}{v_i(s)} = \frac{v_o(s)}{v_1(s)} . \frac{v_1(s)}{v_i(s)}$

$= \left(1 + \frac{R_f}{R_i}\right)\frac{sRC}{1+sRC}$ {using eqs. (1) and (2)}

$= \frac{sA_oRC}{1+sRC}$ ..... (3)

Where $A_o = 1 + \frac{R_f}{R_i}$

Standard form of Transfer Function:

Let $\omega_l = \frac{1}{RC}$

Then from eq. (3), we can write

$$H(s) = \frac{sA_oRC}{1+sRC} = \frac{\frac{sA_o}{\omega_l}}{\frac{s}{\omega_l}+1} = \frac{A_o s}{s+\omega_l} \quad \ldots\ldots\ (4)$$

Frequency Response:

To determine the frequency response put s = jω in eq. (3). Then we get

$$H(j\omega) = \frac{A_o}{1+\frac{1}{sRC}}$$

$$= \frac{A_o}{1+\frac{1}{j\omega RC}}$$

$$= \frac{A_o}{1+\frac{1}{j2\pi fRC}} \qquad (\text{Since } \omega = 2\pi f)$$

$$= \frac{A_o}{1-\frac{j}{2\pi RC}.\frac{1}{f}} \qquad (\text{Since } \frac{1}{j} = -j)$$

$$= \frac{A_o}{1-j\frac{f_l}{f}} \quad \ldots\ldots\ (5)$$

Where $f_l = \frac{1}{2\pi RC}$ or $\omega_l = \frac{1}{RC}$

Consider eq. (5).

When $f \gg f_l$, $|H(j\omega)| = \frac{A_o}{1-j.0} = 0$

When $f = f_l$, $|H(j\omega)| = \frac{A_o}{\sqrt{1^2+1^2}} = \frac{A_o}{\sqrt{2}}$

When $f \ll f_l$, $|H(j\omega)| = \frac{A_o}{1-j.\infty} = 0$

Fig. 3(b) shows the frequency response of first order LPF.

Important observations in Fig. 3(b):

i. Maximum gain is A_o at f = 0 Hz.
ii. At f_l, gain falls by ,707A_o (or – 3 dB below A_o when A_o is expressed in dB).
iii. Frequency response from 0 to f_l is called stop band.
iv. When $f < f_l$, gain decreases at a rate of 20 dB/decade.
v. Range of frequencies $> f_l$ is called pass band

SECOND ORDER LPF AND HPF

In 1st order LPF and HPF, the gain rolls off at a rate of -20 dB/decade. i.e., response is not close to ideal response. For 2nd order LPF and HPF roll off rate is - 40 dB/decade.

Let us consider a general 2nd order filter (it is called Sallen-key filter) as shown in Fig. 4. Let us derive expression for $\frac{v_o}{v_i}$. Then we can substitute appropriate values for Y1, Y2, Y3, and Y4 to get the expression for $\frac{v_o}{v_i}$ for (a) 2nd order LPF (b) 2nd order HPF.

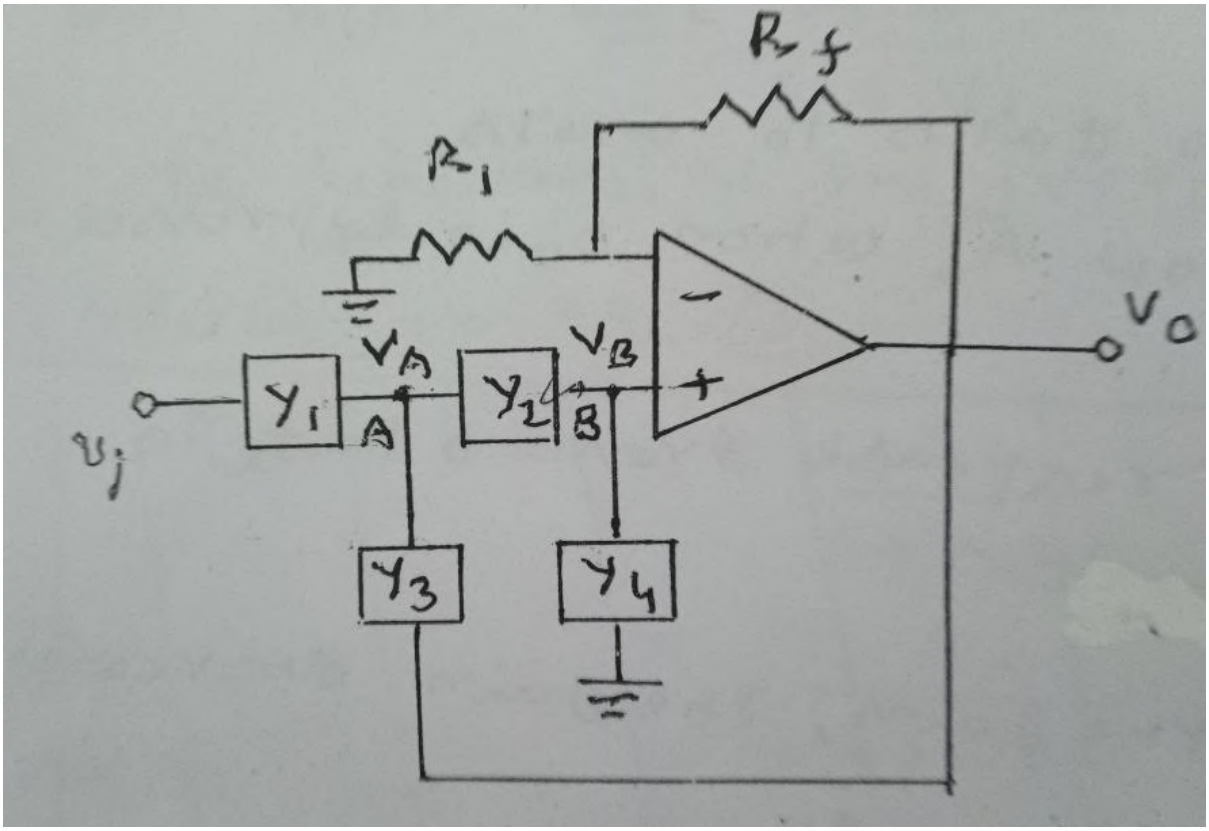


Fig. 4: Sallen-Key Filter

Let v_A be the voltage at node A and v_B ne the voltage at node B.

Since opamp is in non-inverting configuration, closed loop gain A_o is given by

$A_o = \frac{v_o}{v_B} = 1 + \frac{R_f}{R_i}$ ….. (1)

i.e., $v_B = \frac{v_o}{A_o}$ ……(2)

Applying KCL at node A, we get

$(v_A - v_i)Y_1 + (v_A - v_B)Y_2 + (v_A - v_o)Y_3 = 0$

i.e., $v_A (Y_1 + Y_2 + Y_3) - v_i Y_1 - v_B Y_2 - v_o Y_3 = 0$

i.e., $v_i Y_1 = v_A (Y_1 + Y_2 + Y_3) - v_B Y_2 - v_o Y_3$

$= v_A\,(Y_1 + Y_2 + Y_3) - \frac{v_o}{A_o} Y_2 - v_o Y_3$ {using eq. (1)}

$= v_A\,(Y_1 + Y_2 + Y_3) - \frac{v_o}{A_o}(Y_2 + A_o Y_3)$ …….. (3)

Applying KCL at node B, we get

$(v_B - v_A)Y_2 + (v_B - 0)Y_4 = 0$

i.e., $-v_B Y_2 + v_B(Y_2 + Y_4) = 0$

i.e., $v_A = \frac{v_B(Y_2+Y_4)}{Y_2}$

$= \frac{v_o}{A_o}\frac{Y_2+Y_4}{Y_2}$ …… (4) {using eq. (2)}

Putting v_A value from eq. (4) into eq. (3), we get

$v_i Y_1 = \frac{v_o}{A_o}\left(\frac{Y_2+Y_4}{Y_2}\right)(Y_1 + Y_2 + Y_3) - \frac{v_o}{A_o}(Y_2 + A_o Y_3)$

$= \frac{v_o}{A_o Y_2}\{(Y_2 + Y_4)(Y_1 + Y_2 + Y_3) - {y_2}^2 - A_o Y_2 Y_3\}$

$= \frac{v_o}{A_o Y_2}\{Y_1 Y_2 + \cancel{y_2^2} + Y_2 Y_3 + Y_2 Y_3 + Y_2 Y_3 + Y_2 Y_3 - \cancel{y_2^2} - A_o Y_2 Y_3\}$

$= \frac{v_o}{A_o Y_2}\{Y_1 Y_2 + Y_4\,(Y_1 + Y_2 + Y_3) + Y_2 Y_3\,(1 - A_o)\}$

$\therefore \frac{v_o}{v_i} = \frac{A_o Y_1 Y_2}{Y_1 Y_2 + Y_4\,(Y_1+Y_2+Y_3) + Y_2 Y_3\,(1 - A_o)}$ ….. (5)

(a) Second order LPF:

To get second order LPF, choose $Y_1 = Y_2 = \frac{1}{R}$ and $Y_3 = Y_4 = SC$. Then Fig. 4 becomes Fig. 5.

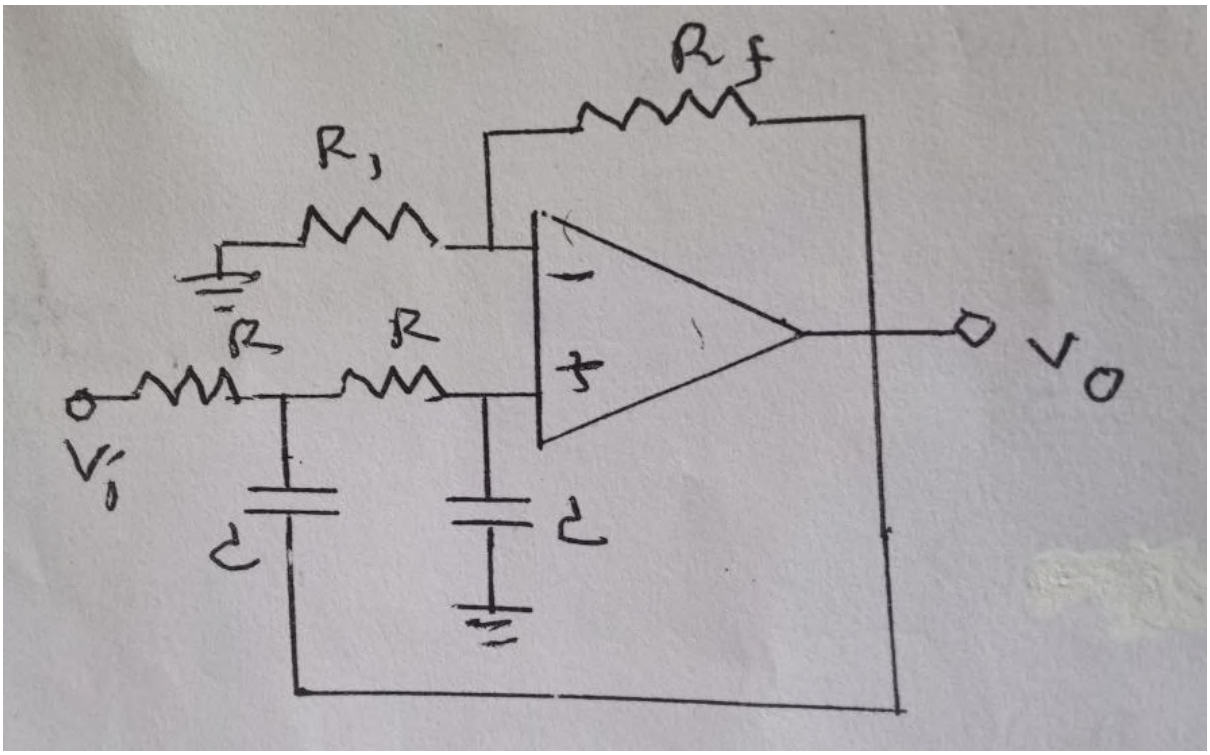


Fig. 5: Second order LPF

Substituting $Y_1 = Y_2 = \frac{1}{R}$ and $Y_3 = Y_4 = SC$ in eq. (5), we get

$$H(s) = \frac{A_o * \frac{1}{R} * \frac{1}{R}}{\frac{1}{R} * \frac{1}{R} + sC\left(\frac{1}{R} + \frac{1}{R} + sC\right) + \frac{1}{R}.sC\ (1 - A_0)}$$

$$= \frac{A_o / R^2}{\frac{1}{R^2} + \frac{sC}{R}(2 + sRC) + \frac{sC}{R}(1 - A_0)}$$

$$= \frac{\frac{A_o}{R^2}}{\frac{1 + sRC\ (2 + sRC) + sRC\ (1 - A_o)}{R^2}}$$

$$= \frac{A_o}{s^2R^2C^2 + sRC\ (3 - A_o) + 1} \quad \ldots\ldots\ldots \quad (6)$$

$s = 0 \Rightarrow H(s) = A_o$

$s = \infty \Rightarrow H(s) = 0$

So,it is an LPF of 2nd order.

For any second order systems such as electrical, mechanical, hydraulic andchemical system, the Transfer function (TF) is given by

$$H(s) = \frac{A_o \omega_h{}^2}{s^2 + \alpha\ \omega_h\ s + \omega_h{}^2} \quad \ldots\ldots (7)$$

Where α = damping factor or damping coefficient

A_o = Gain of the system

$\omega_h = 2\pi f_h$, where f_h =Highest cutoff frequency.

Eq. (6) can be written as

$$H(s) = \frac{{}^{A_O}/_{R^2C^2}}{s^2+\frac{sRC}{R^2C^2}(3-A_o)+\frac{1}{R^2C^2}}$$

$$= \frac{{}^{A_O}/_{R^2C^2}}{s^2+\frac{s}{RC}(3-A_o)+\frac{1}{R^2C^2}} \quad \ldots\ldots\ldots (8)$$

Comparing eqs. (7) and (8), we get

$\omega_h = \frac{1}{RC}$ and $\alpha = 3 - A_o$

Where $\alpha = 1.414 = \sqrt{2}$ for Butterworth filter, 1.06 for Chebyshev filter and 1.73 for Bessel filter.

Normalized expression for Transfer function:

Putting $s = j\omega$ in eq. (7), we get

$H(j\omega) = \frac{A_o {\omega_h}^2}{(j\omega)^2+\alpha\,\omega_h\, s(j\omega)+{\omega_h}^2}$ Dividing the numerator and denominator of above equation by ${\omega_h}^2$, we get

$$H(j\omega) = \frac{A_o}{(j\omega/\omega_h)^2+j\,\alpha\,\omega\,\omega_h/{\omega_h}^2+1}$$

$$= \frac{A_o}{(j\omega/\omega_h)^2+j\,\alpha\,\omega/\omega_h+1} \quad \ldots\ldots\ldots (9)$$

$$= \frac{A_o}{{s_n}^2+j\,\alpha\,s_n+1}$$

Where s_n = normalized frequency = $j\left(\frac{\omega}{\omega_h}\right)$

Expression for magnitude of TF in dB:

Eq. (9) can be written as

$$H(j\omega) = \frac{A_o}{-(\omega/\omega_h)^2+j\,\alpha\,\omega/\omega_h+1}$$

$$= \frac{A_o}{\left(1-\frac{\omega^2}{{\omega_h}^2}\right)+j\,\alpha\frac{\omega}{\omega_h}}$$

$$20 \log |H(j\omega)| = 20 \log \frac{A_o}{\sqrt{\left(1-\frac{\omega^2}{\omega_h{}^2}\right)^2 + \alpha^2 \frac{\omega^2}{\omega_h{}^2}}}$$

$$= 20 \log \frac{A_o}{\sqrt{1+\frac{\omega^4}{\omega_h{}^4} - 2\frac{\omega^2}{\omega_h{}^2} + \alpha^2 \frac{\omega^2}{\omega_h{}^2}}}$$

Since α^2 =2, last 2 terms in the root get cancelled. So, we get

$$20 \log |H(j\omega)| = \frac{A_o}{\sqrt{1+\frac{\omega^4}{\omega_h{}^4}}} = \frac{A_o}{\sqrt{1+\left(\frac{\omega}{\omega_h}\right)^4}}$$

$$= \frac{A_o}{\sqrt{1+\left(\frac{f}{f_h}\right)^4}} \qquad \text{(since } \omega = 2\,\pi\, f \text{ and } \omega_h = 2\,\pi\, f_h$$

Generalized expression for magnitude of TF for LPF is

$$20 \log |H(j\omega)| = \frac{A_o}{\sqrt{1+\left(\frac{f}{f_h}\right)^{2n}}}$$

Where 'n' is the order of the filter.

(b) Second order HPF:

Consider the expression for $\frac{v_o}{v_i}$ derived using general second order filter.

$$\frac{v_o}{v_i} = \frac{A_o Y_1 Y_2}{Y_1 Y_2 + Y_4\,(Y_1 + Y_2 + Y_3) + Y_2 Y_3\,(1 - A_o)} \quad \ldots\ldots (5)$$

To get second order LPF, choose $Y_1 = Y_2 = sC$ and $Y_3 = Y_4 = \frac{1}{R}$. Then Fig. 4 becomes Fig. 6.

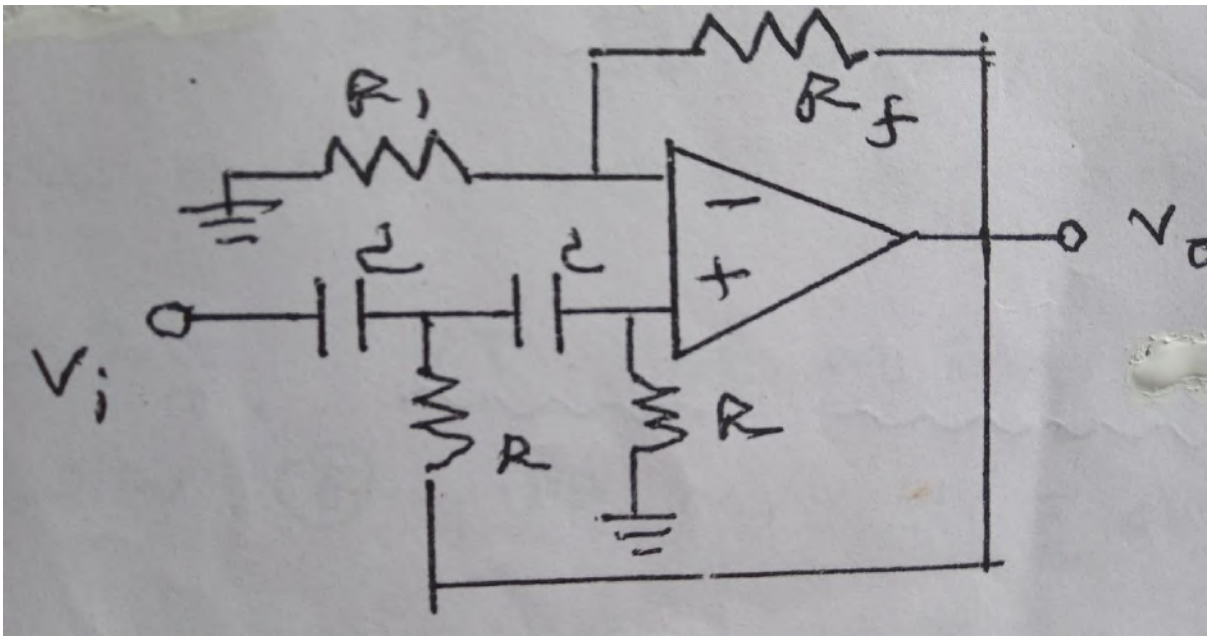


Fig. 6: Second order HPF

Substituting $Y_1 = Y_2 = \frac{1}{R}$ and $Y_3 = Y_4 = SC$ in eq. (5), we get

$$H(s) = \frac{A_o * sC*sC}{sC*sC + \frac{1}{R}\left(sC+sC+\frac{1}{R}\right) + \frac{sC}{R}(1-A_0)}$$

$$= \frac{A_o\, s^2C^2}{s^2C^2 + \frac{sC}{R}\left(2+\frac{1}{sCR}\right) + \frac{sC}{R}(1-A_0)}$$

$$= \frac{A_o}{1+\frac{1}{sRC}\left(2+\frac{1}{sRC}\right) + \frac{1}{sRC}(1-A_o)}$$

$$= \frac{A_o}{1+\frac{1}{sRC}(3-A_o)+\frac{1}{s^2R^2C^2}} \quad \ldots\ldots\ldots \quad (6)$$

For any second order system such as electrical, mechanical, hydraulic andchemical system, the Transfer function (TF) is given by

$$H(s) = \frac{A_o s^2}{s^2+\alpha\,\omega_l\, s+\omega_l{}^2} \quad \ldots\ldots (7)$$

Where α = damping factor or damping coefficient

A_o = Gain of the system

$\omega_l = 2\pi f_l$, where f_l =Lowest cutoff frequency.

Eq. (6) can be written as

$$H(s) = \frac{A_O/R^2C^2}{s^2+\frac{sRC}{R^2C^2}(3-A_o)+\frac{1}{R^2C^2}}$$

$$= \frac{A_o}{1+\frac{\omega_l}{s}(3-A_o)+\frac{{\omega_l}^2}{s}} \quad \ldots\ldots\ldots (8)$$

Comparing eqs. (7) and (8), we get

$\omega_l = \frac{1}{RC}$ and $\alpha = 3 - A_o$

Where $\alpha = 1.414 = \sqrt{2}$ for Butterworth filter, 1.06 for Chebyshev filter and 1.73 for Bessel filter.

Normalized expression for Transfer function:

Putting s = j ω in eq. (8), we get

$H(j\omega) = \frac{A_o}{\left(\frac{\omega_l}{j\omega}\right)^2+\frac{\omega_l}{j\omega}(3-A_o)+1}$ Dividing the numerator and denominator of above

$$= \frac{A_o}{1-\frac{j\omega_l}{\omega}(3-A_o)-\frac{{\omega_l}^2}{\omega^2}} \quad \ldots\ldots\ldots (9)$$

Normalized expression for Transfer function is

$$= \frac{A_o}{{s_n}^2+j\ \alpha\ s_n+1}$$

Where s_n = normalized frequency = $-\frac{j\omega_l}{\omega}$ and $\alpha = 3 - A_o$

Expression for magnitude of TF in dB:

Eq. (9) can be written as

$H(j\omega) = \frac{A_o}{1-\frac{{\omega_l}^2}{\omega^2}-\frac{j\omega_l}{\omega}(3-A_o)}$

$|H(j\omega)| = \frac{A_o}{\sqrt{\left(1-\frac{{\omega_l}^2}{\omega^2}\right)^2+\alpha^2\frac{{\omega_l}^2}{\omega^2}}}$

$20 \log |H(j\omega)| = 20 \log \frac{A_o}{\sqrt{\left(1-\frac{{\omega_l}^2}{\omega^2}\right)^2+\alpha^2\frac{{\omega_l}^2}{\omega^2}}}$

$$= 20 \log \frac{A_o}{\sqrt{1+\frac{{\omega_l}^4}{\omega^4}-2\frac{{\omega_l}^2}{\omega^2}+\alpha^2\frac{\omega^2}{{\omega_h}^2}}}$$

Since α^2 =2, last 2 terms in the root get cancelled. So, we get

$$20 \log |H(j\omega)| = \frac{A_o}{\sqrt{1+\frac{\omega_l^4}{\omega^4}}} = \frac{A_o}{\sqrt{1+\left(\frac{\omega_l}{\omega}\right)^4}}$$

$$= \frac{A_o}{\sqrt{1+\left(\frac{f_l}{f}\right)^4}} \qquad \text{(since } \omega = 2\,\pi\,\text{f and } \omega_l = 2\,\pi\,f_l$$

Generalized expression for magnitude of TF for LPF is

$$20 \log |H(j\omega)| = \frac{A_o}{\sqrt{1+\left(\frac{f_l}{f}\right)^{2n}}}$$

Where 'n' is the order of the filter.

Design of LPF and HPF:

(a) Design of second order LPF:

Select equal values of R and C in the two RC sections. Then follow the steps given below.

Step1: Choose value of f_h. (e.g.: f_h = 1000 Hz)

Step2: Select C Value $\leq$ 0.1 μF (Say C = 0.1 μF)

Step3: Calculate R value using the relation

$$f_h = \frac{1}{2\pi RC}$$

Step4: Select R_i and R_f using the relation

$$A_0 = 1 + \frac{R_f}{R_i} = 3 - \alpha$$

Where A_o = Pass band gain

A = Damping factor

= 1.414 for Butterworth filter

= 1.06 for Chebyshev filter

= 1.73 for Bessel filter

(b) Design of second order HPF:

Follow the same procedure given above, where cutoff frequency 'f_h' is replaced by f_l, where f_l is the lower cutoff frequency of HPF.

Note: Use mylar or tantalum capacitors.

Design of first order LPF and HPF:

Procedure is same as that of second order LPF and HPF. But here there is a single RC section.

Problem1: Design a 2nd order Butterworth LPF having upper cutoff frequency of 1 KHz.

Solution:

Given $f_h = \frac{1}{2\pi RC}$ = 1 KHz = 1000 Hz

i.e., $R = \frac{1}{2\pi fC} = \frac{1}{2\pi \text{ x } 1000 \text{ x } C}$

Choose C = 0.1 μF = 10^{-7} F $\frac{R_f}{R_i}$

$\therefore R = \frac{1}{2\pi \text{ x } 1000 \text{ x } 10^{-7}}$

We know that $A_o = 3 - \alpha$

For Butter worth filter $\alpha = \sqrt{2} = 1.414$

$\therefore A_o = 3 - 1.414 = 1.586$

But $A_o = 1 + \frac{R_f}{R_i}$

i.e., $1.586 = 1 + \frac{R_f}{R_i}$

or $\frac{R_f}{R_i} = 1.586 - 1 = 0.586$

Let R_f = 5.86 KΩ

Then $R_i = \frac{5.86 \text{ K}\Omega}{0.586}$ = 10 KΩ

Problem2: Design a 2nd order Butterworth LPF having lower cutoff frequency of 1 KHz.

Solution is same as in Problem1. Answers are also same.

But frequency response formulae are different for LPF and HPF.

Band Pass Filter (BPF)

A BPF allows a particular band of frequencies and rejects frequencies outside that band.

Wide Band Pass Filter:

Let f_l = Lower cutoff frequency

f_h = Higher cutoff frequency

f_o = Center frequency

Q = Quality Factor

Then

$$f_o = \sqrt{f_l f_h}$$

Bandwidth = $f_h - f_l$

$$Q = \frac{f_o}{f_h - f_l}$$

There are two types of BPFs. They are wide BPF and narrow BPF. For wide BPF, Q < 10 and for narrow BPF, Q > 10.

Wide Band Pass Filter (Q < 10)

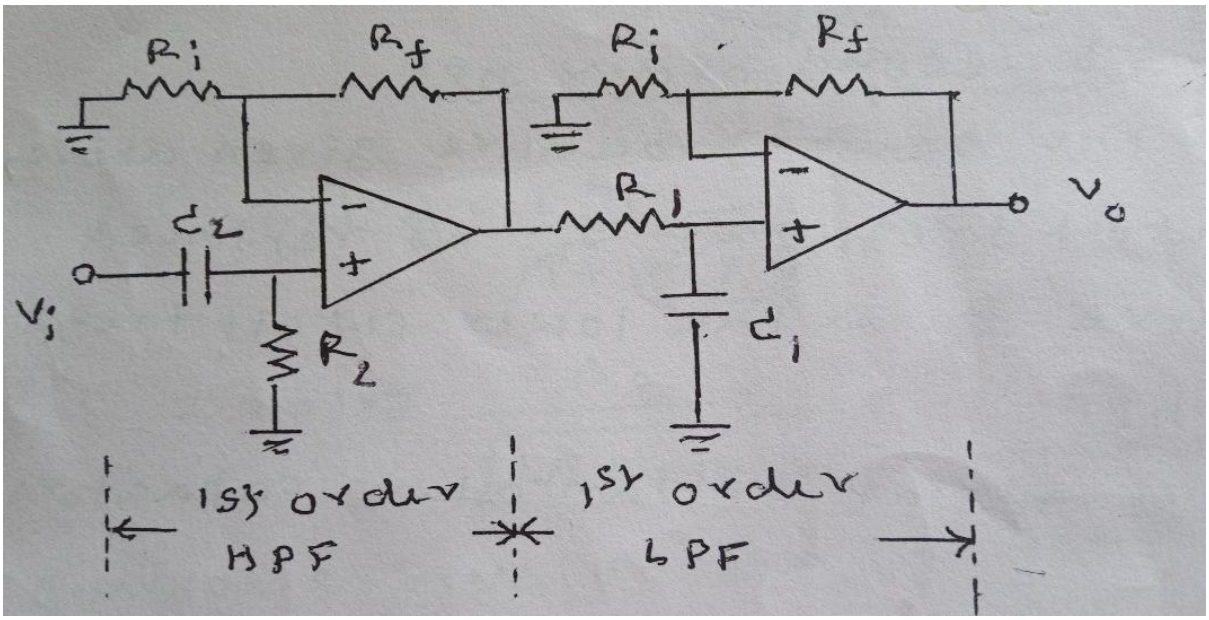


Fig. 7: First order wide BPF

Fig. 7 represents a first order wide BPF. It is obtained by cascading a first order HPF and a first order LPF as shown.

Let A_{o1} = Pass band gain of HPF

Let A_{o2} = Pass band gain of LPF

Then

Magnitude of Transfer Function (TF) of HPF is given by

$| H_{HP}| = \frac{A_{01}}{\sqrt{1+\left(\frac{f_l}{f}\right)^2}}$ where $f_l = \frac{1}{2\pi R_2 C_2}$ …… (1)

Magnitude of Transfer Function (TF) of HPF is given by

$| H_{LP}| = \frac{A_{o2}}{\sqrt{1+\left(\frac{f}{f_h}\right)^2}}$ where $f_h = \frac{1}{2\pi R_1 C_1}$ …… (2)

Magnitude of TF of BPF =

$| H_{BP}| = | H_{HP}| * | H_{LP}|$ ……. (3)

Eqs. (1), (2) and (3), we write

$| H_{BP}| = \frac{A_{01}}{\sqrt{1+\left(\frac{f_l}{f}\right)^2}} \frac{A_{o2}}{\sqrt{1+\left(\frac{f}{f_h}\right)^2}} = \frac{A_0}{\sqrt{1+\left(\frac{f_l}{f}\right)^2 1+\left(\frac{f}{f_h}\right)^2}}$ where $A_o = A_{o1}.A_{o2}$

…….. (4)

Problem 3: Design a wide band pass filter having f_l = 400 Hz and f_h = 2 KHz with a pass band gain of 2.

Solution:

For LPF:

f_h = 2 KHz = 2000 Hz = $\frac{1}{2\pi R_1 C_1}$

Choose C_1 = 0.01 μF = 0.01 x 10^{-6} F

Then $R_1 = \frac{1}{2\,\pi\ x\ 2000\ x\ 0.01\ x\ 10-6}$ = 7.9 KΩ

For LPF:

f_l = 400 Hz = $\frac{1}{2\pi R_2 C_2}$

Choose C_2 = 0.01 μF = 0.01 x 10^{-6} F

Then $R_2 = \frac{1}{2\,\pi\ x\ 400\ x\ 0.01\ x\ 10-6}$ = 39.8 KΩ

Here, the pass band gains of LPF and HPF should be same.

Let $A_{o1} = A_{o2} = 2 = 1 + \frac{R_f}{R_i}$

i.e., $R_f = R_i$ = 10 KΩ (say)

$f_o = \sqrt{f_h f_l} = \sqrt{2000\ x\ 400} = 894.4$ KΩ

$Q = \frac{f_o}{BW} = \frac{f_o}{f_h - f_l} = \frac{894.4}{2000-400} = 0.56$

Note that Q < 10

Narrow Band Pass Filter:

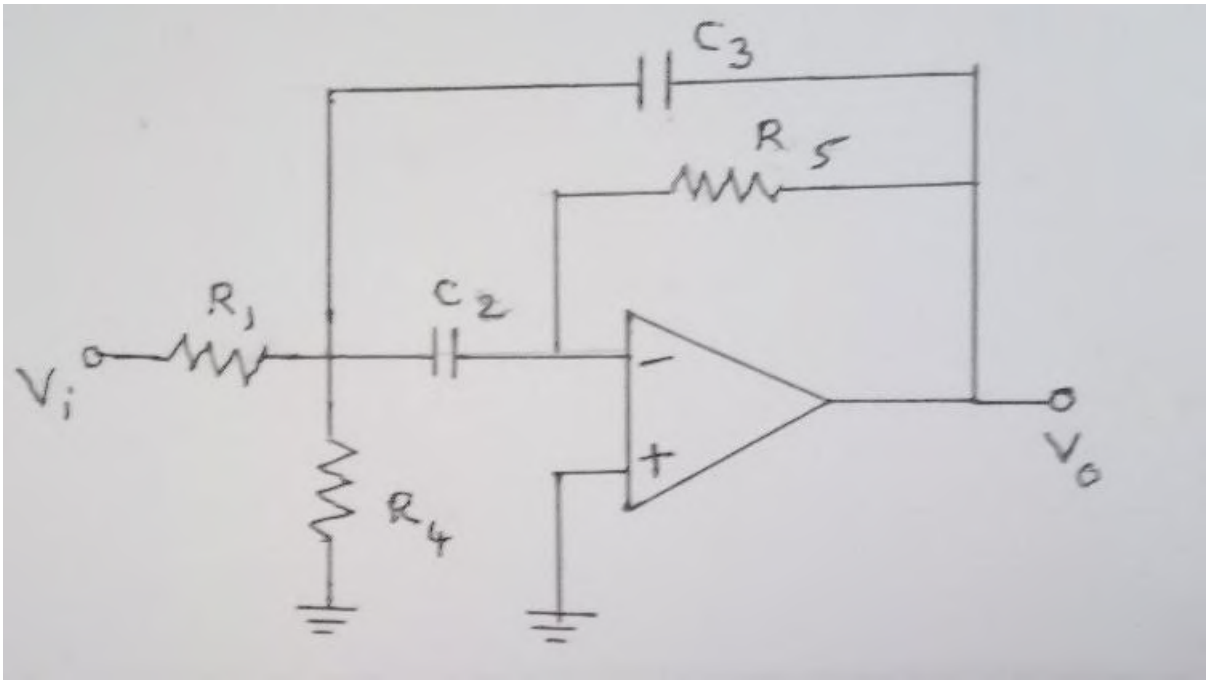


Fig. 8: Second Order narrow Band Pass Filter

Fig. 8 shows a narrow BPF. Here Q > 10.

BAND REJECT FILTER (BRF):

A BRF is also called a band stop filter or band elimination filter. It rejects a particular band of frequencies and rejects frequencies outside this band. There are two types of BRF. They are wide BRF and narrow BRF.

Wide Band Reject Filter:

It has a Q < 10. It can be made using an LPF, HPF and a summer. Its necessary constraints are (i) The lower cutoff frequency f_l of the HPF >> the higher cutoff frequency f_h of LPF. (ii) The pass band gains of LPF and HPF should be same.

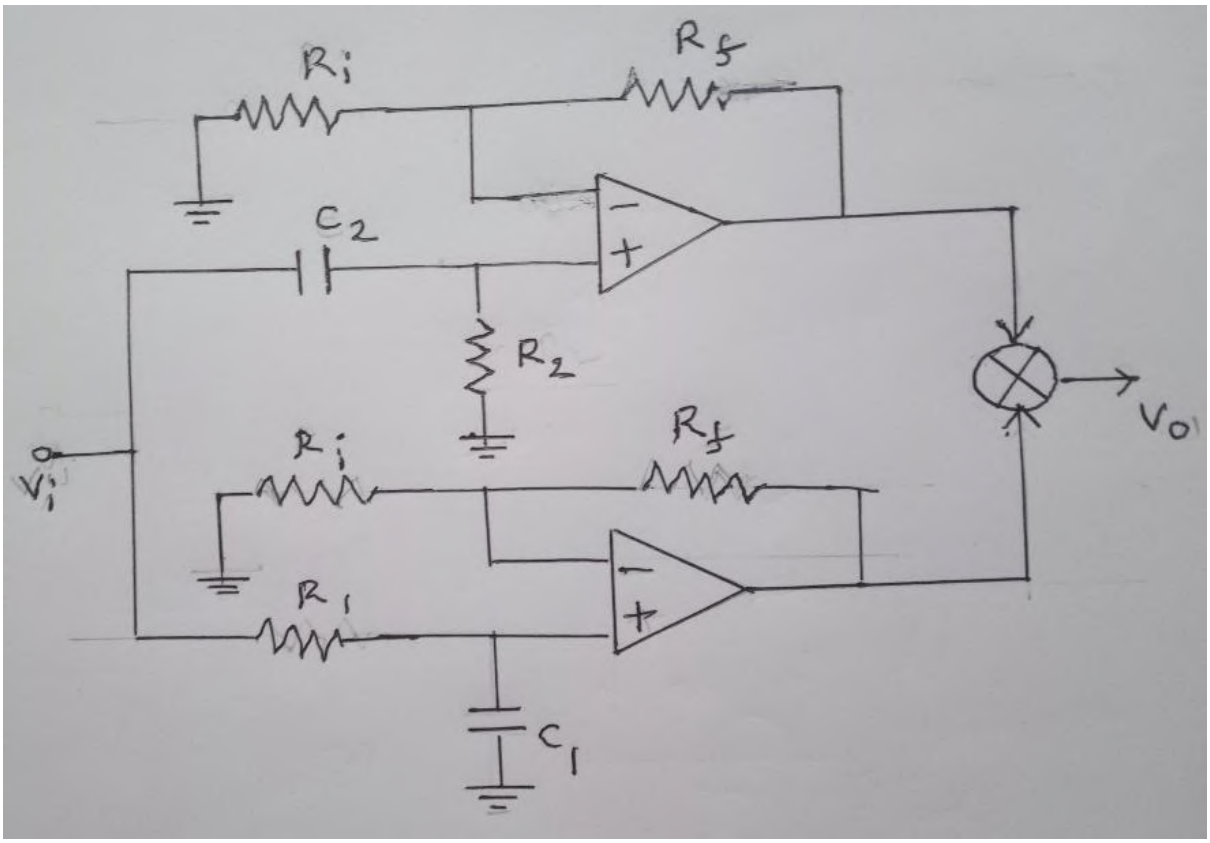


Fig. 9 (a): Wide BRF

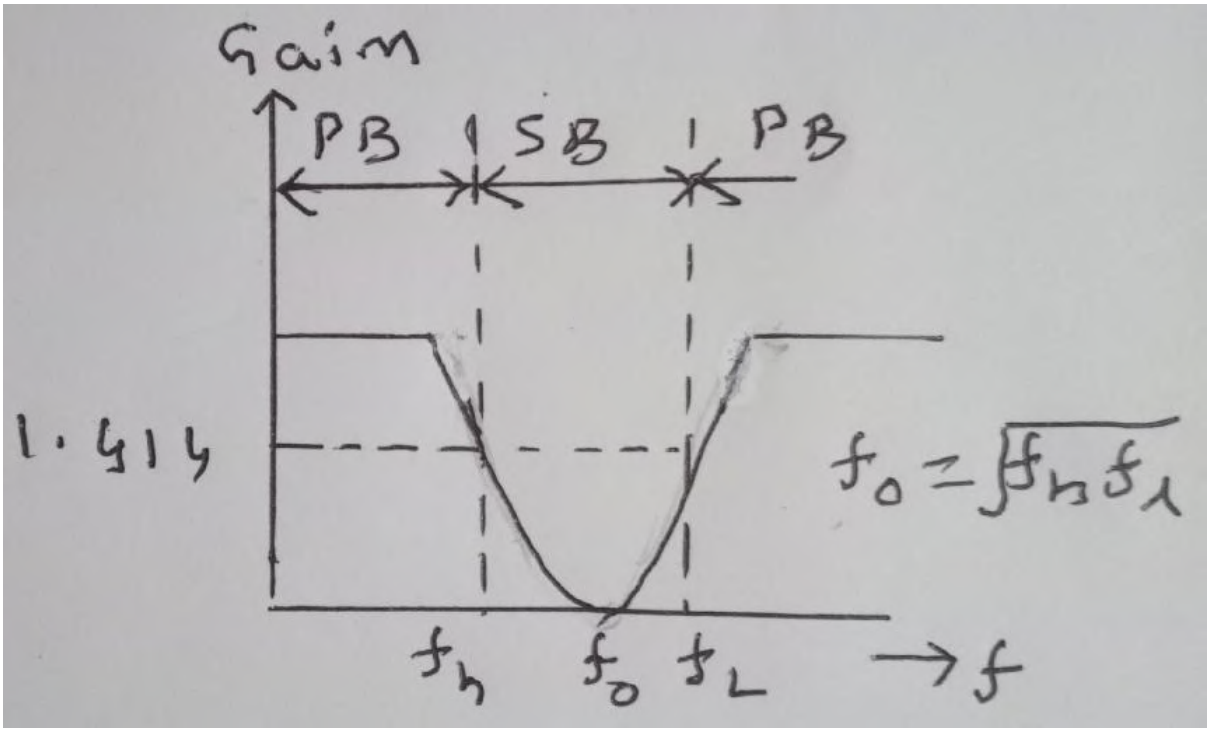


Fig. 9 (b): Frequency response of wide BRF

Fig. 9 (a) shows the circuit diagram of a wide BRF. Fig. 9 (b) shows its frequency response.

Problem 4: Design a wide band reject filter having f_h = 400 Hz and f_l = 2 KHz with a pass band gain of 2.

Solution:

For HPF:

f_l = 2 KHz = 2000 Hz = $\frac{1}{2\pi R_2 C_2}$

Choose C_2 = 0.1 μF = 0.1 x 10^{-6} F

Then R_2 = $\frac{1}{2\,\pi\ x\ 2000\ x\ 0.1\,x\,10-6}$ = 795 Ω ≈ 800 Ω

For LPF:

f_h = 400 Hz = $\frac{1}{2\pi R_1 C_1}$

Choose C_1 = 0.1 μF = 0.1 x 10^{-6} F

Then R_1 = $\frac{1}{2\,\pi\ x\ 400\ x\ 0.1\,x\,10-6}$ = 3978 Ω ≈ 4 KΩ

Here, the pass band gains of LPF and HPF should be same.

Let $A_{o1} = A_{o2}$ = 2 = $1 + \frac{R_f}{R_i}$

i.e., $R_f = R_i$ = 10 KΩ (say)

Narrow Band Reject Filter:

Narrow BRF is commonly called a **notch filter.** It is useful for the rejection of a single frequency like 50 Hz power line hum.

There are mainly two ways of realizing notch filter

First way of realizing a second order notch filter:
It is achieved by cascading a second order narrow BPF and a summer. It is shown in Fig. 10 (a)

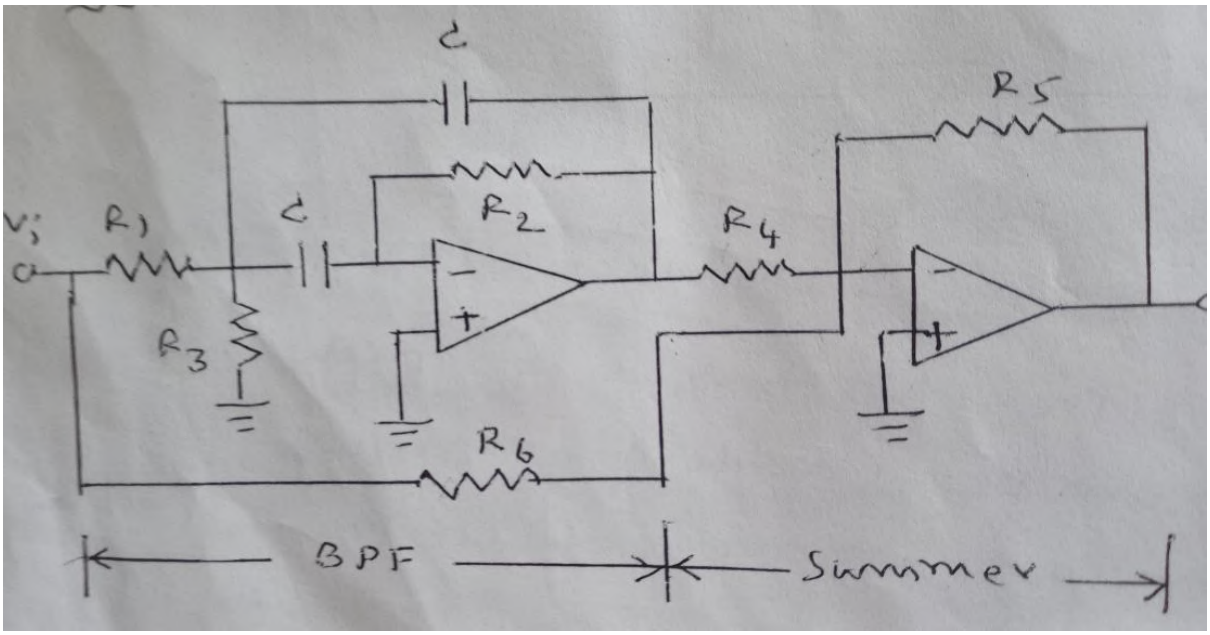


Fig. 10 (a)

Second way of realizing a second order notch filter (Twin-T filter):

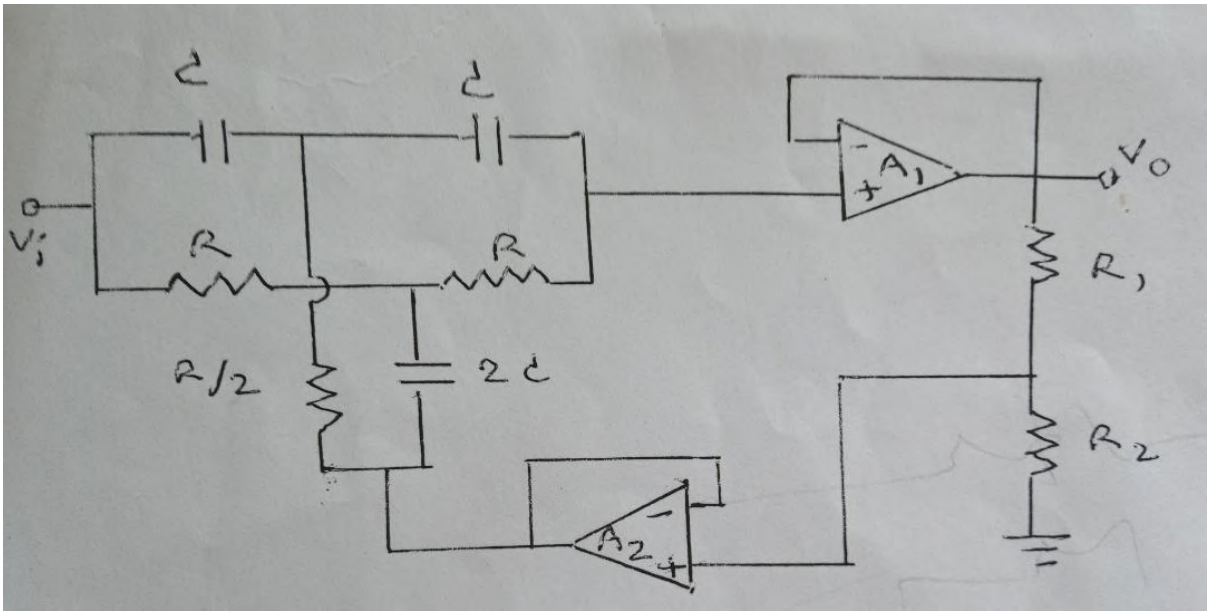


Fig. 10 (b) Twin-T notch filter

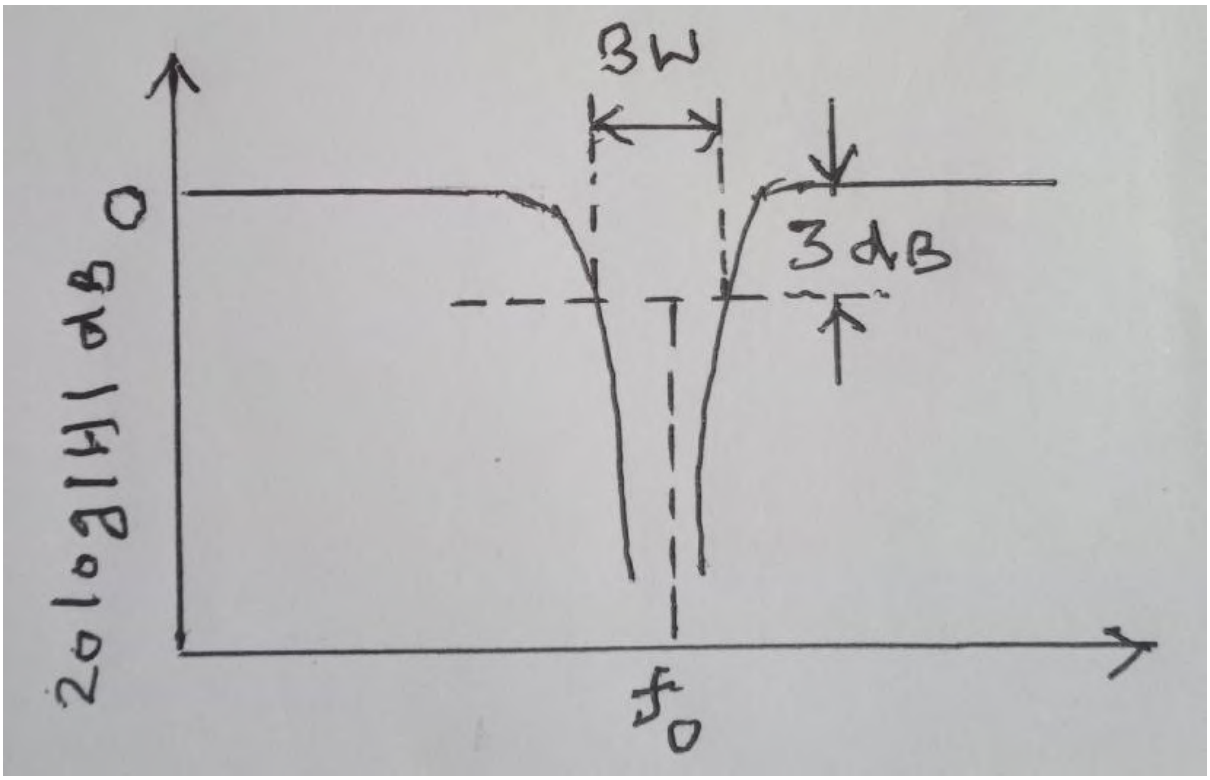


Fig. 10 (c) Frequency response of notch filter

Fig. 10 (b) shows a Twin-T notch filter.

If f_l = Lower cutoff frequency

f_h = Higher cutoff frequency

f_o = Center frequency

Q = Quality Factor

From the analysis of the circuit, we can show that

$$f_o = \frac{1}{2\pi RC}$$

Bandwidth = BW = $f_h - f_l = 4 f_o (1 - K)$

$$Q = \frac{f_o}{BW} = \frac{1}{4-K}$$

As K approaches unity, Q factor becomes very large and bandwidth approaches 0. Mismatches between resistors and capacitors also limit the value of Q and bandwidth.

R_1 and R_2 are used to adjust gain of the filter.

Fig. 10 (c) shows the frequency response of notch filter.

Problem 5: Design a 50 Hz active notch filter.

Solution:

Consider the Twin-T filter in Fig. 10 (b)

Given that $f_o = \frac{1}{2\pi RC}$ = 50 Hz

Let C = 0.1 μF = 0.1 x 10^{-6} F

Then R = $\frac{1}{2\pi f_o C}$

= $\frac{1}{2\pi \times 50 \times 0.1 \times 10^{-6}}$ = 31.8 KΩ

For R/2, we can use two 31.8 KΩ in parallel.

For 2C, we can use two capacitors in parallel.

ALL PASS FILTERS (APFs)

All pass filters (APFs) allow all frequency components of input signal without any attenuation. Their main advantage is they provide desired phase shift at any frequency. Thus, APFs are used in phase correction in analog systems (e.g.: Analog telephone systems).

APFs are also called delay equalizers or phase correctors.

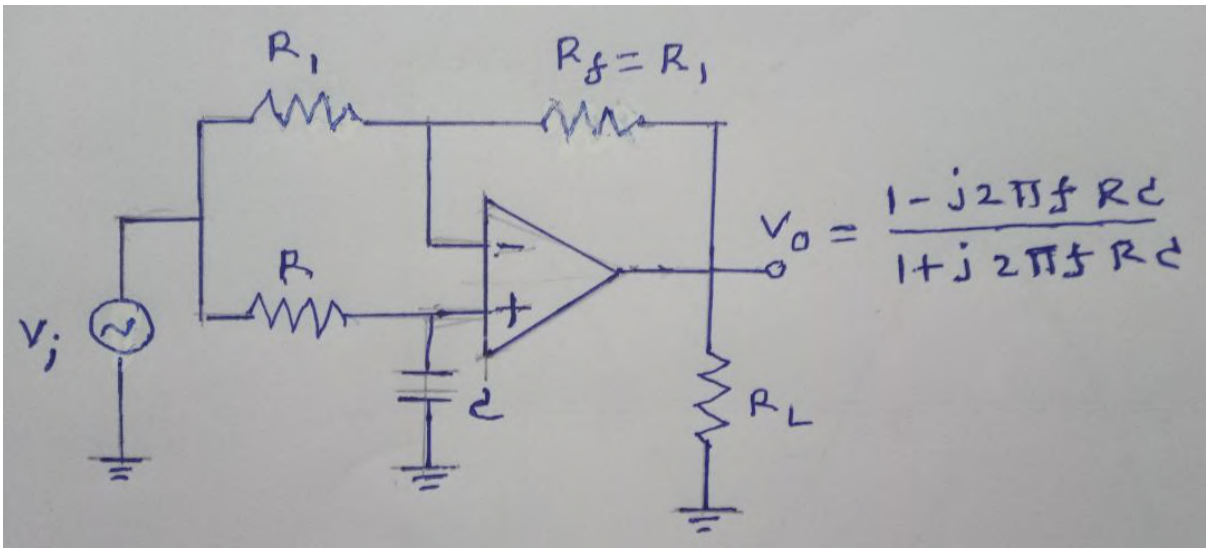


Fig. 11 (a) All Pass Filter

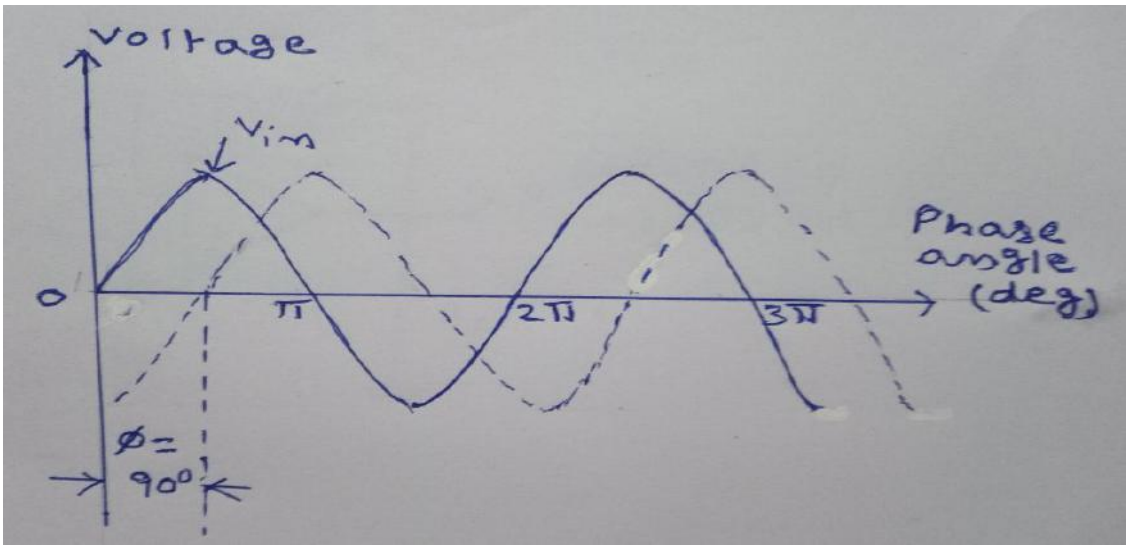


Fig. 11 (b) Waveforms of All Pass Filter

Fig. 11 (a) shows an All Pass Filter where v_i is input voltage and v_o is output voltage and R_f = R_1. Fig. 11 (b) shows waveforms for All Pass Filter.

Let the voltage at node 'a' is v_a.

By using super position theorem, we can write

$$v_o = - \frac{R_f}{R_1} . v_i + (1 + \frac{R_f}{R_1}) v_a$$

Since $R_f = R_1$. above equation becomes

$$v_o = - v_i + 2v_a \quad \ldots . (1)$$

But $v_a = v_i . \frac{\frac{1}{sC}}{R+\frac{1}{sC}} = v_i . \frac{1}{1+sRC}$ ..... (2)

Eqs. (1) and (2) ⇒

$$v_o = - v_i + 2v_i . \frac{1}{1+sRC}$$

$$= v_i \left(-1 + \frac{2}{1+sRC} \right)$$

$$= v_i \frac{(-1-sRC+2)}{1+sRC}$$

$$= v_i \frac{1-sRC}{1+sRC}$$

$$= v_i \frac{1-j\omega RC}{1+j\omega RC}$$

i.e., $\frac{v_o}{v_i} = \frac{1-j\omega RC}{1+j\omega RC}$

$= \frac{1-j\,2\pi fRC}{1+j\,2\pi fRC}$

∴ Magnitude of $\frac{v_o}{v_i}$ is given by

$$\left|\frac{v_o}{v_i}\right| = \frac{\sqrt{1+(2\pi f RC)^2}}{\sqrt{1+(2\pi f RC)^2}} = 1$$

i.e., $|v_o| = |v_i|$ for all frequencies.

The phase shift Φ between v_o and v_i is given by

$\Phi = -\tan^{-1}(2\pi fRC) - \tan^{-1}(2\pi fRC)$

$= -2\tan^{-1}(2\pi fRC)$

Thus, the phase shift can be varied with frequency for a given R and C.

We can obtain phase shift from 0 to 1800 as we change the frequency from 0 to ∞.

As phase shit here is negative, the output v_o lags input v_i .

The phase shift can be made positive by interchanging R and C in Fig. 11 (a)

*****

555 TIMER (Introduction)

- A 555 timer is a monolithic IC that can produce accurate and highly stable time delays or oscillations.
- It operates with supply range of + 5 V and produces a delay ranging from‘μsecs’ to hours.
- It is compatible with TTL and CMOS logic circuits.
- It is available as an 8-pin metal can, an 8-pin mini-DIP or 14-pin DIP.

Applications of 555 timer:

1. Monostable multivibrator
2. Astable multivibrator
3. Waveform (Pulse, ramp and square waves) generator
4. Burglar and toxic alarms
5. Voltage regulators
6. Traffic control
7. Digital logic probes
8. Temperature measurement and control
9. Infrared transmitters.

PIN Diagram of 555 timer:

Fig. 1 (a) represents the pin diagram of a 555 timer.

Here R and C are external resistor and capacitor. Let us assume that the width of trigger pulse is very small.

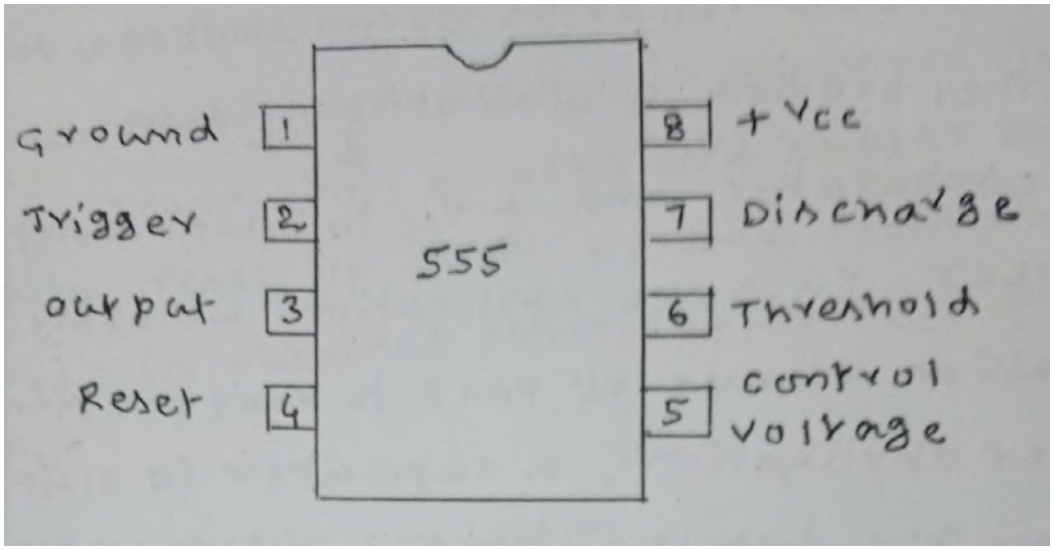


Fig. 1 (a): Pin diagram of 555 Timer

Functional diagram of a 555 timer:

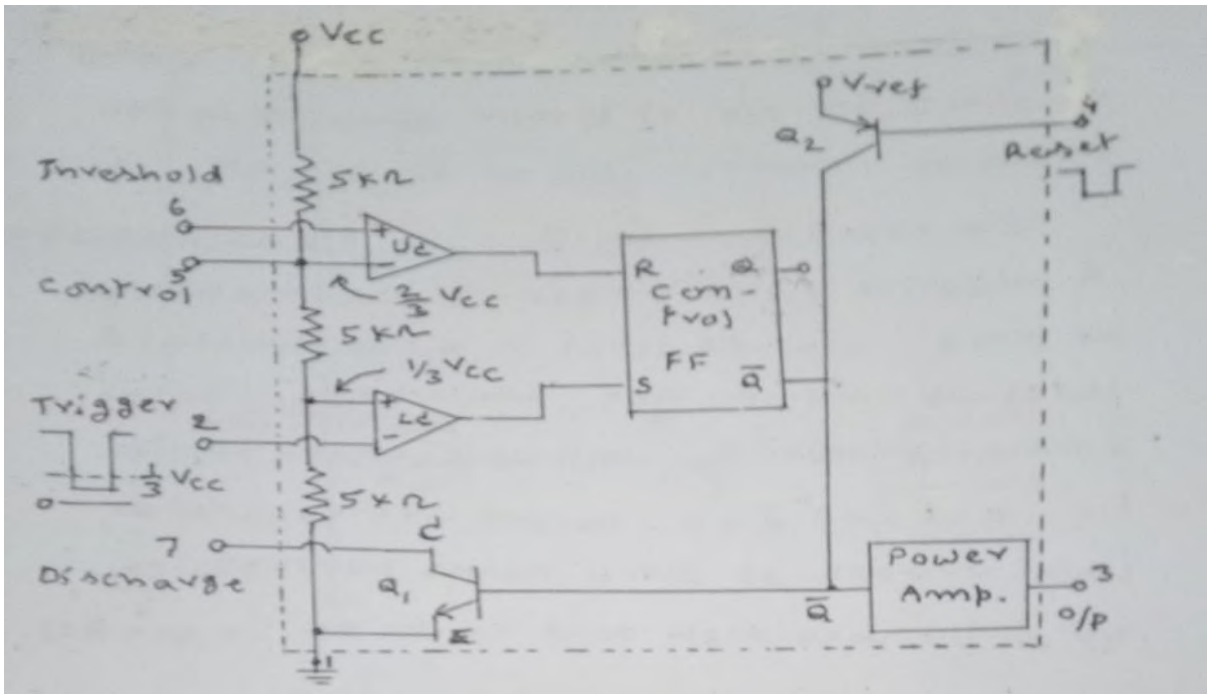


Fig. 1 (b): Functional diagram

Fig. 1 (b) shows its functional diagram.Three 5 KΩ resistors form voltage divider. They provide a bias of $\frac{2}{3}$ V_{CC} to the **upper comparator (UC)** and $\frac{1}{3}$ V_{CC} to the **lower comparator (LC)**. In some applications, we apply modulation voltage at pin 5 to vary the time. In other applications, a capacitor (0.01μF) is connected between pin 5 and ground to by-pass noise or ripple from the supply. Q and Q' are outputs of control Flip-Flop**(FF)**. Outputs of **UC and LC** are R and S inputs of FF respectively. **Power amplifier** is basically an inverter. Its output at pin 3 is output of timer. Since Q' is the input of inverter, output at pin 3 is Q.

In standby mode, Q=0, Q' = 1. So, o/p at pin 3 = Q = 0. A negative going triggering pulse is applied at pin 2. Its dc level is > the threshold level of **LC** (i.e., $\frac{1}{3}$ V_{CC}). When trigger pulse passes through $\frac{V_{CC}}{3}$, output of **LC** goes high and sets the **FF**. i.e., Q = 1 and Q' = 0. During + ve excursion, when voltage at pin 6 passes through $\frac{2}{3}$ $V_{CC,}$ o/p of **UC** goes high and resets the **FF**. i.e., Q = 0 and Q' = 1.

Reset input at pin 4 is used to reset the FF, irrespective of o/p of **LC**. This input is < 0.4 V. When the reset input is not used, it is connected to V_{CC}.

Transistor Q_2 acts as a buffer and isolates reset i/p from FF and transistor Q_1. V_{ref} is applied from supply V_{CC}. It drives Q_2.

MONOSTABLE OPERATION USING 555 TIMER

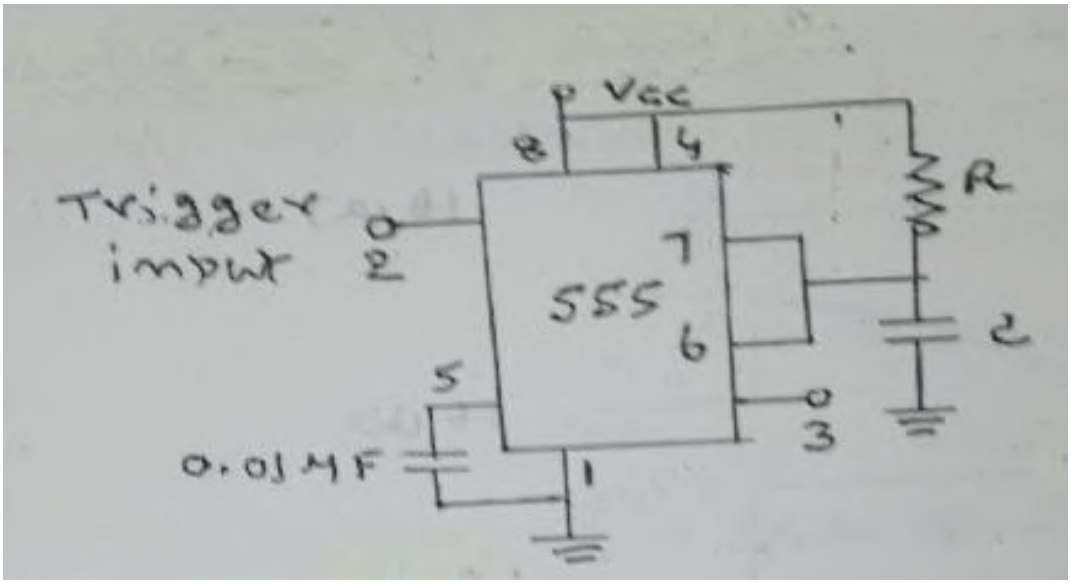


Fig. 2 (a):Pin Connections for Monostable multivibrator

Fig. 2 (a) shows the timer with required connections for monostable operation and Fig. 2 (b) shows the functional diagram. Fig. 3 shows different waveforms of the circuit.

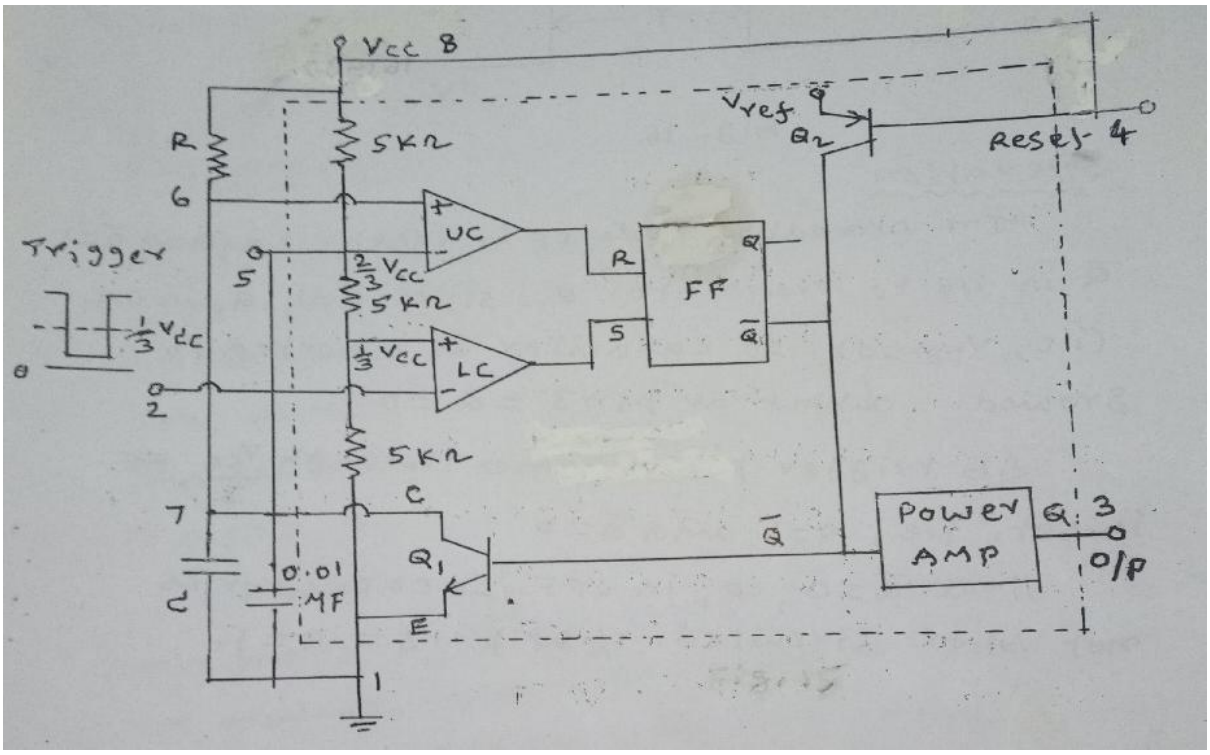


Fig.2 (b) Functional Diagram for Monostable multivibrator

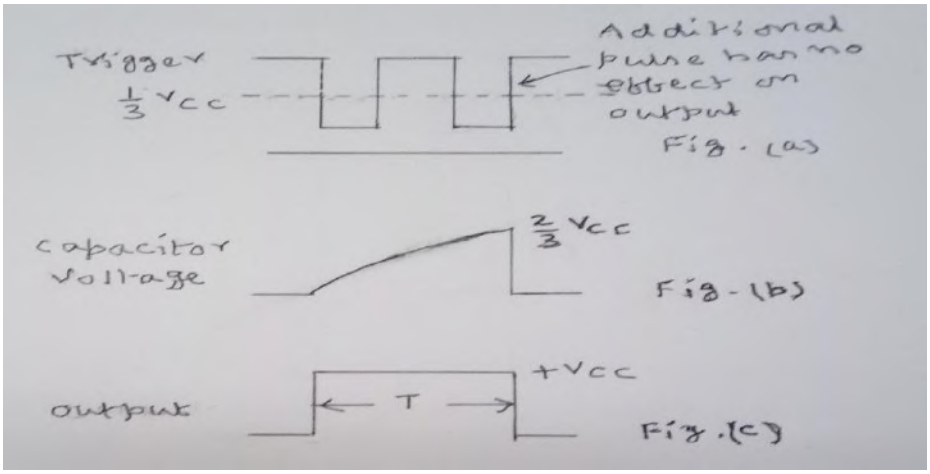


Fig. 3: Waveforms of Monostable multivibrator

In standby mode, FF is reset. i.e., Q = 0 and Q' = 1. Here Q' is the input to transistor Q_1. Since Q' = 1, Q_1 is ON (i.e., $V_{CE} = 0$). So, capacitor is shorted to ground. Output at pin 3 = Q = 0.

Fig. 3(a) shows the triggering pulse.

As trigger pulse passes through $\frac{V_{CC}}{3}$, FF is set. i.e., Q = 1 and Q' = 0.

Since Q' = 0, Q_1 is OFF. So, capacitor is not short circuited (i.e., capacitor is unclamped). Output at pin 3 = Q = 1.

The timing cycle begins now.

Now C charges exponentially through R towards V_{CC}, with a time constant RC as shown in Fig. 3 (b).

After a time T (say), capacitor voltage v_c is just $>\frac{2}{3} V_{CC}$. So, UC resets the FF. i.e., Q = 0 and Q' = 1.

Since Q' = 0, Q_1 is ON. Then C discharges rapidly to ground potential.

The o/p returns to standby state or ground potential as shown in Fig.3 (c)

If a second trigger pulse is given as shown in the right side of fig. 3(a), before T, it has no effect on the operation of the circuit.

Derivation for Output Pulse Width 'T':

We know that capacitor charge equation is given by

v_c (t) = $v_f + (v_i - v_f) e^{-t/RC}$ ..... (1)

where v_i = Initial voltage = 0

v_f = Final (target) voltage = V_{CC}

∴ Eq. (1) becomes

v_c (t) = $V_{CC} + (0 - V_{CC}) e^{-t/RC}$

= $V_{CC} (1 - e^{-t/RC})$ ..... (2)

At t = T, v_c (t) = $\frac{2}{3} V_{CC}$

∴ Eq. (2) becomes

$\frac{2}{3} V_{CC} = V_{CC} (1 - e^{-T/RC})$

i.e., $e^{-T/RC} = 1 - \frac{2}{3} = \frac{1}{3}$

or $e^{T/RC}$ = ln (3)

i.e., T = RC ln (3)

i.e., **T = 1.1 RC seconds**

Applications of Monostable Multivibrator:

1. Frequency Divider
2. Pulse Stretcher
3. Pulse Width Modulation (PWM)
4. Linear Ramp Generator

Problem 1: Design a monostable multivibrator using 555 Timer, shown in Fig. 2 (b) with a pulse width of 100 m Sec.

Solution:

Given $T = 1.1\ RC = 100 \times 10^{-3}$ Sec

Choose $R = 100\ K\Omega = 10^5\ \Omega$

Then $100 \times 10^{-3} = 1.1 \times 10^5 \times C$

$$\therefore\ C = \frac{100\ x\ 10^{-3}}{1.1\ x\ 10^5} = 0.909\ \mu F = 1\ \mu F$$

ASTABLE OPERATION USING 555 TIMER

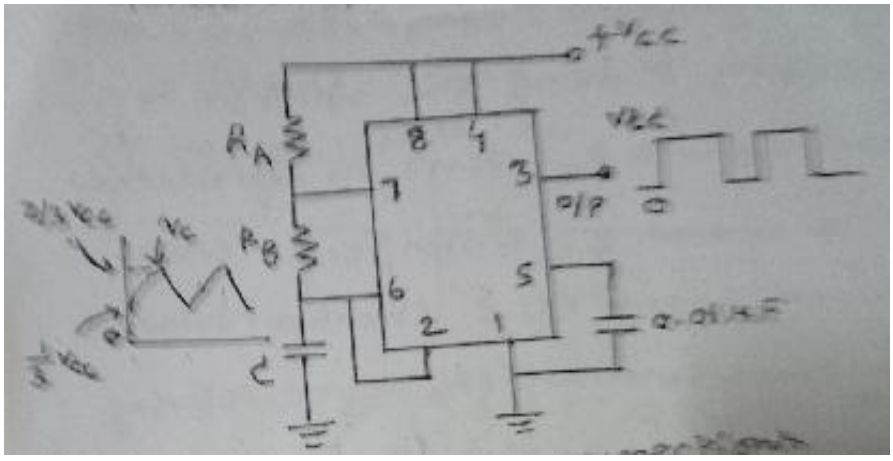


Fig. 4 (a): Pin Connections for Astable operation

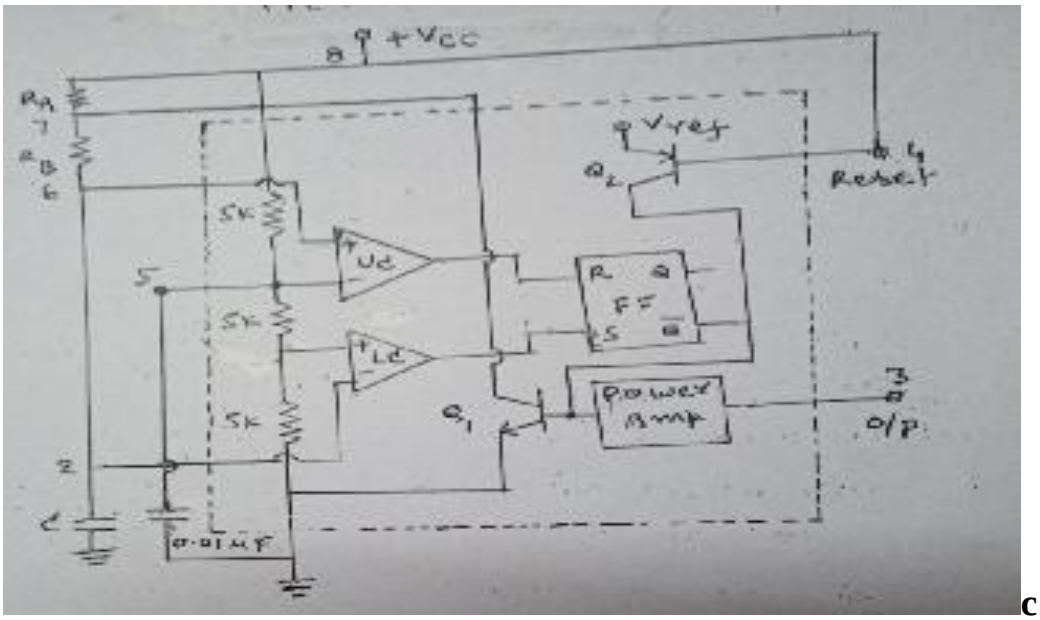


Fig. 4 (b): Functional Diagram for Astable Operation

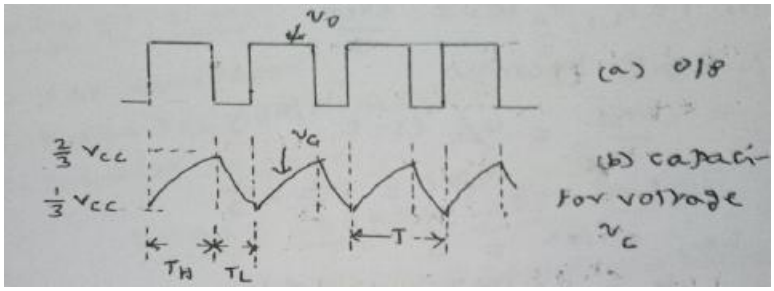


Fig. 5 (a) and (b): Waveforms of Astable Multivibrator

Fig. 4 (a) represents the pin connection diagram for 555 timer in astable mode. R_A and R_B are external resistors and C is external capacitor. Fig. 4 (b) shows the functional diagram. Compared to monostable operation, timing resistor R is split into two sections R_A and R_B. Pin 7 (collector of Q_1) is connected to the junction of A and B. When V_{CC} is connected, external capacitor C charges towards V_{CC}through R_A and R_B, with a time constant of (R_A + R_B) C. During this time output at pin 3 = High (i.e., Q = 1 and Q' = 0). Since Q' = 0, C is unclamped.

When v_c is just $>\frac{2}{3} V_{CC}$, Upper comparator (UC) resets FF. i.e., Q = 0 and Q' = 1. So Q_1 is **ON**(V_{CE} = 0) and C discharges through R_B with a time constant R_BC.

For better operation R_A and R_B are taken large to limit current.

During discharging, when v_c is just $<\frac{V_{CC}}{3}$, lower comparator (LC) sets the FF. i.e., Q = 1 and Q' = 0. So Q_1 is OFF ($V_{CE} = V_{CC}$) and C is unclamped. Thus, C is charged and discharged periodically between $\frac{2\,V_{CC}}{3}$ and $\frac{V_{CC}}{3}$ respectively.

Fig. 5 (a) and Fig. 5 (b) shows the waveforms of output and voltage v_c across capacitor respectively.

Derivation for Time Period 'T' of Output:

We know that capacitor charge equation is given by

v_c (t) = $v_f + (v_i - v_f)e^{-t/RC}$ ….. (1)

where v_i = Initial voltage

v_f = Final (target) voltage

Let t_H = Time taken for C to charge from $\frac{V_{CC}}{3}$ *to* $\frac{2\,V_{CC}}{3}$ = $t_1 - t_2$

Where t_1 = Time taken to charge from 0 to $\frac{2\,V_{CC}}{3}$

and t_2 = Time taken to charge from 0 to $\frac{V_{CC}}{3}$

Let t_L = Time taken for C to discharge from $\frac{2\,V_{CC}}{3}$ to $\frac{V_{CC}}{3}$

For t_1, v_i = 0 and v_f = V_{CC}.

∴ Eq. (1) becomes

v_c (t) = $V_{CC} + (0 - V_{CC})\, e^{-t/RC}$

= $V_{CC}\,(1 - e^{-t/RC})$ …… (2)

At t = t_1, v_c (t) = $\frac{2}{3}\,V_{CC}$

∴ Eq. (2) becomes

$\frac{2}{3}V_{CC} = V_{CC}\,(1 - e^{-t_1/RC})$

i.e., $e^{-t_1/RC} = 1 - \frac{2}{3} = \frac{1}{3}$

or $e^{t_1/RC}$ = ln (3)

i.e., t_1 = RC ln (3)

i.e., t_1 = 1.1 RC

For t_2, v_i = 0 and v_f = V_{CC}.

∴ Eq. (1) becomes

v_c (t) = V_{CC} + (0 – V_{CC}) $e^{-t/RC}$

= V_{CC} (1 – $e^{-t/RC}$) …… (3)

At t = t_2, v_c (t) = $\frac{V_{CC}}{3}$

∴ Eq. (3) becomes

~~V_{CC}~~/3= ~~V_{CC}~~ (1 – $e^{-t_2/RC}$)

i.e., $e^{-t_2/RC} = 1 - \frac{1}{3} = \frac{2}{3}$

i.e., $e^{t_2/RC} = \frac{3}{2}$

Taking logarithms on both sides, we get

i.e., t_2 = RC ln ($\frac{3}{2}$)

i.e., t_2 = 0.405 RC

∴ $t_H = t_1 - t_2$ = 1.1 RC – 0.405 RC

= 0.69 RC (where R = R_A + R_B)

Thus $\mathbf{t_H}$ = **0.69 ($\mathbf{R_A}$ + $\mathbf{R_B}$)** ….. (4)

For t_L, $v_i = \frac{2\,V_{CC}}{3}$, v_f = 0

∴ Eq. (1) becomes

v_c (t) = 0 + ($\frac{2\,V_{CC}}{3}$ – 0) $e^{-t/RC}$

= $\frac{2\,V_{CC}}{3}\,e^{-t/RC}$ ….. (5)

At t = t_L, v_c (t) = $\frac{V_{CC}}{3}$

∴ Eq. (5) becomes

~~V_{CC}~~/~~3~~= (2 ~~V_{CC}~~ /~~3~~) $e^{-t_L/RC}$

i.e., $e^{-t_L/RC} = \frac{1}{2}$

i.e., $e^{t_L/RC} = 2$

Taking logarithms on both sides, we get

$t_L/_{RC}$ = ln (2)

i.e., t_L = RC ln (2) = 0.69 RC

Here R = R_B

$\therefore t_L = 0.69\ R_B C$.... (6)

$\therefore$ T = $t_H + t_L$

i.e., **$T = 0.69\ (R_A + 2R_B)\ C$**{from eqs. (4) and (6)}

Frequency = $\frac{1}{T} = \frac{1}{0.69\ (R_A + 2R_B)\ C} = \frac{1.45}{(RA + 2RB)\ C}$

% Duty cycle = $\frac{t_L}{t_L + t_H}$ x 100%

$= . \frac{0.69\ R_B \cancel{C}}{0.69\ (R_A + 2R_B)\cancel{C}}$

$= \frac{R_B}{(R_A + 2R_B)}$ **x 100%**

Problem 2: For the astable multivibrator in Fig. 4 (b), R_A = 6.8 KΩ, R_B = 3.3 KΩ and C = 0.1 μF. Calculate t_{HIGH}, t_{LOW}, free running frequency and duty cycle.

Solution:

t_{HIGH} = 0.69 (R_A + 2 R_B)

= 0.69 (6.8 x 10^3 + 2 x 3.3 X 10^3) x 0.1 10^{-6}

= 0.7 mSec

t_{LOW}= t_L = 0.69 R_B C

= 0.69 x 3.3 x 10^3 x 0.1 x 10^{-6}

= 0.23 mSec

f = $\frac{1.45}{(R_A + 2\ R_B)\ C} = \frac{1.45}{(6.8 \text{ x } 10^3 + 2 \text{ x } 3.3 \text{ x } 10^3) \text{ x } 0.1 \text{ x } 10^{-6}}$

= 1.07 KHz

Duty cycle = $\frac{R_B}{(R_A + 2R_B)}$

$= \frac{3\ x\ 10^3}{6.8\ x\ 10^3 + 2\ x\ 3.3\ x\ 10^3} = 0.25$

% Duty cycle = 25%

Applications of Astable Multivibrator:

1. FSK Generator
2. Pulse Position Modulator (PPM)
3. Schmitt Trigger

555 timer as Schmitt Trigger:

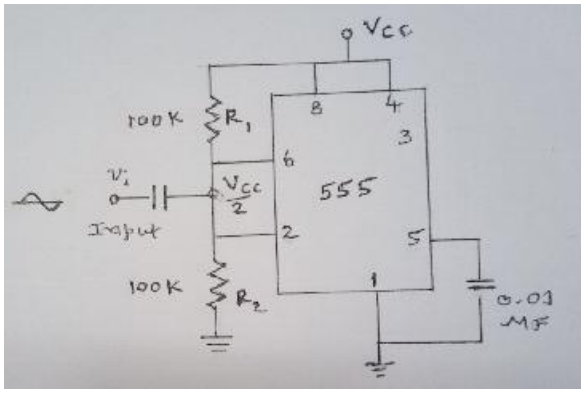


Fig. 6: 555 timer in Schmitt trigger operation

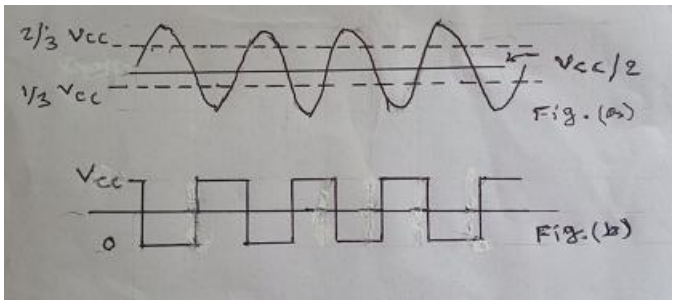


Fig. 7:Inputand OutputWaveforms

Fig. 6shows the pin connections of 555 timer used as a Schmitt trigger. Here the two comparators are tied together and externally biased at $V_{CC}/2$ through R_1 and R_2 as shown. We know that Upper comparator trips at$\frac{2\,V_{CC}}{3}$and lower comparator trips at $\frac{V_{CC}}{3}$. The bias provided by R_1 and R_2 is cantered between these two limits. Now a sine wave is applied. If its amplitude exceeds ($\frac{2\,V_{CC}}{3}$ - $\frac{V_{CC}}{3}$) reference levels, the internal FF sets and resets alternately and provides a square wave as shown in Fig. 7(a) andFig. 7 (b) show the i/p signal. Here frequency of square wave is same as that of input signal.

PHASE LOCKED LOOPS (PLLs)

Phase Locked Loop (PLL) is an important block of linear systems. PLLs were first used in 1930s in communication applications. Previously, they were costly because they were realized in discrete form. Now PLLs are available as inexpensive ICs.

Principle of Operation of PLL:

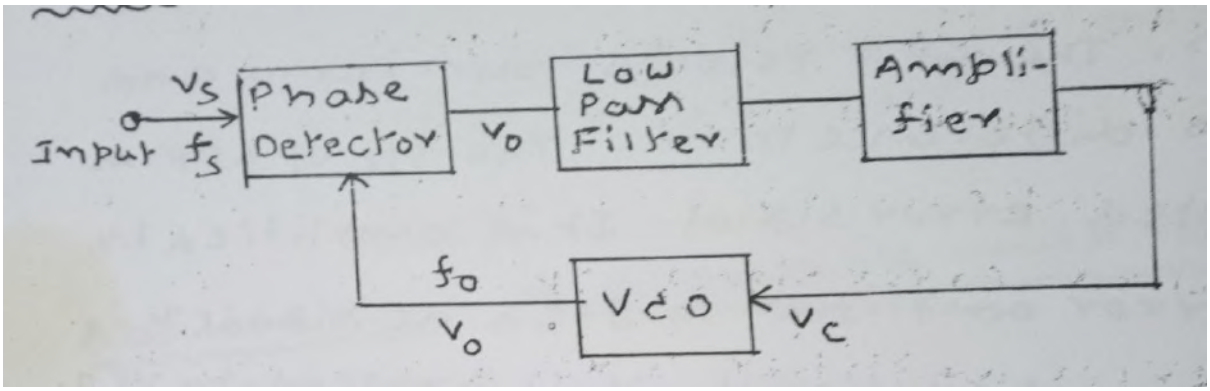


Fig. 8: Block diagram of PLL

Fig. 8 represents the block diagram of a PLL. It consists of a phase detector, Low Pass Filter (LPF), an amplifier and a Voltage Controlled Oscillator (VCO).

Let v_s = Input voltage

f_s = Input frequency

v_o = Output voltage

f_o = Output frequency

Before i/p signal is applied, PLL is said to be in **free-running mode**. When i/p signal v_s of frequency f_s is applied to PLL, the phase detector (or mixer) compares the phase and frequency of v_s to that of the output v_o of VCO. If the 2 signals differ in frequency or phase angle, it generates an error voltage v_c.

The phase detector is basically a multiplier circuit. Its o/p mainly consists of sumterm (f_s + f_o) and difference term (f_s - f_o). The LPF rejects sum term and allow difference term. The o/p of LPF is called **error signal**. It is amplified by the error amplifier to get a dc signal 'v_c' called **control signal**. This v_c is applied to VCO. It shifts the VCO frequency in a direction to reduce the difference between f_s and f_o. Once this action starts, PLL is said to be in **capture state**. The VCO frequency f_o continues to change until it equals the i/p frequency f_s. Then PLL is said to be in **locking state**. When locking occurs, the loop tracks any change in f_s.

Now the phase difference between i/p and o/p signals generates a corrective voltage v_c to shift the VCO frequency from f_o to f_s.

Important definitions related to PLL:

1. Lock-in range: It is the range of frequencies over which the PLL can maintain lock with the incoming signals.

2. Capture range: It is the range of frequencies over which the PLL can acquire lock with the i/p signals.

3. Pull-in time: It is the total time taken by PLL to establish lock.

More details (Short notes) on lock-in range and capture range:

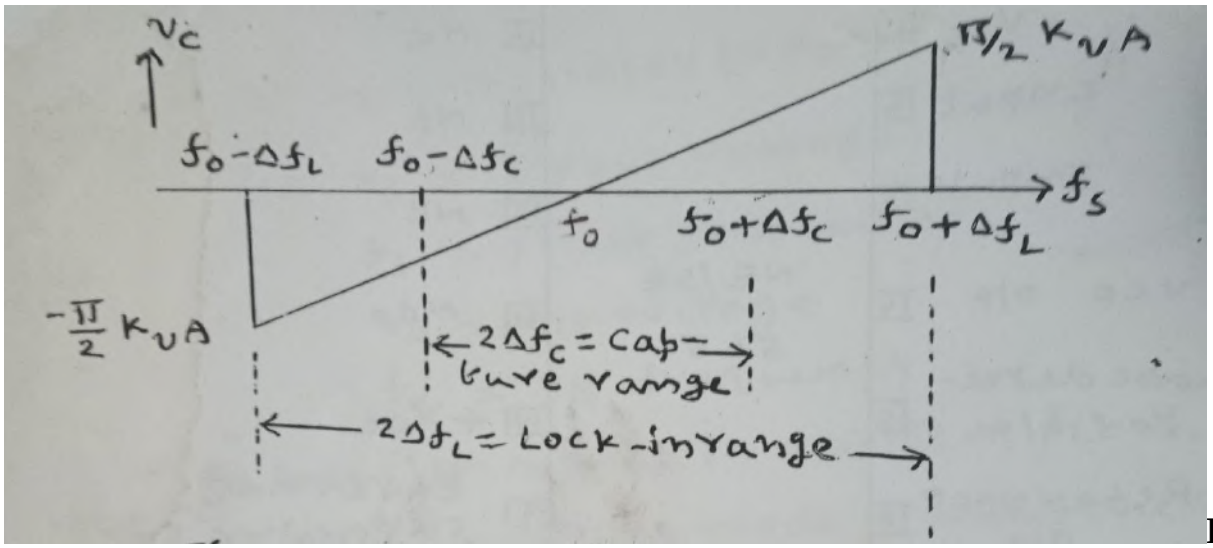


Fig. 9: Lock-in range and capture range of PLL

Let us consider a monolithic IC with analog phase detector.

Its **lock-in range** is given by

$$\mathbf{2\ \Delta f_L = k_v\ k_\Phi A\ \pi}$$

Where k_v = Voltage to frequency transfer coefficient of PLL **(Hz/Volt)**

k_Φ= Phase angle to voltage transfer coefficient of PLL **(Volt/Radian)**

and A = Voltage gain of amplifier

Its **capture range** is given by

$$\mathbf{2\ \Delta f_C = 2\ \sqrt{f_1.\ \Delta f_L}}$$

Where $f_1 = \frac{1}{2\pi RC}$ = 3 dB frequency of LPF

$2\ \Delta f_L$= Total lock-in range

Fig. 9 shows the lock-in range $2\ \Delta f_L$and capture range $2\ \Delta f_C$. Both ranges are expressed in % age of f_o. Both ranges are symmetrically located w.r.t. VCO frequency f_o. **Lock-in range is always > capture range.**

We need large capture range. But large capture range will make the PLL more susceptible to noise.

COMPONENTS OF PLL

- **Phase Detector (Phase comparator, or Mixer or multiplier circuit)**
- **Low Pass Filter**
- **Amplifier**
- **Voltage Controlled Oscillator**

Phase Detector:

Phase detector compares the phase and frequency of incoming signal v_s to that of output $v_o$of VCO.Its o/p mainly consists of sum term ($f_s + f_o$) and difference term ($f_s - f_o$). Output of phase detector is fed to the LPF.

There are 2 types of phase detectors: analog and digital. Abalanced modulator is used as analog phase detector. An XOR gate serves as a digital phase detector.

Most of the monolithic PLL ICs use analog phase detectors. For discrete PLLs, digital phase detectors are preferred because of their simplicity.

Low Pass Filter:

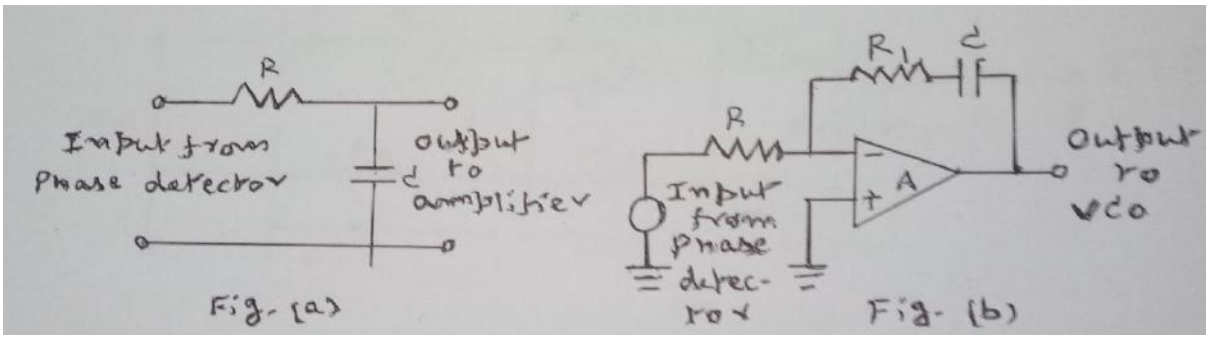


Fig.10: Low Pass Filter of PLL

Low pass filter removes the high frequency components and noise. It also controls the dynamic characteristics of the PLL such as lock-in and capture ranges, bandwidth and transient response.

If filter bandwidth is reduced, the response time increases. But it also reduces the capture range.

This produces a high noise immunity and locking stability.

Amplifier:

It is used to amplify the error signal, i.e., o/p of LPF.

Voltage Controlled Oscillator:

Initially when no input signal is given to PLL, it runs with a free running frequency f_o. When input is given, PLL action starts. Then v_c is the o/p of amplifier. It is a dc control voltage.

This v_c is applied to VCO. It shifts the VCO frequency in a direction to reduce the difference between f_s and f_o. Once this action starts, PLL is said to be in capture state. The VCO frequency f_o continues to change until it equals the i/p frequency f_s. Then PLL is said to be in locking state. When locking occurs, the loop tracks any change in f_s.

Now the phase difference between i/p and o/p signals generates a corrective voltage v_c to shift the VCO frequency from f_o to f_s.

MONOLITHIC PLL IC (NE/SE 565)

IC PLL 565 is available as a 14-pin DIP package andas a 10-pin metal can package.

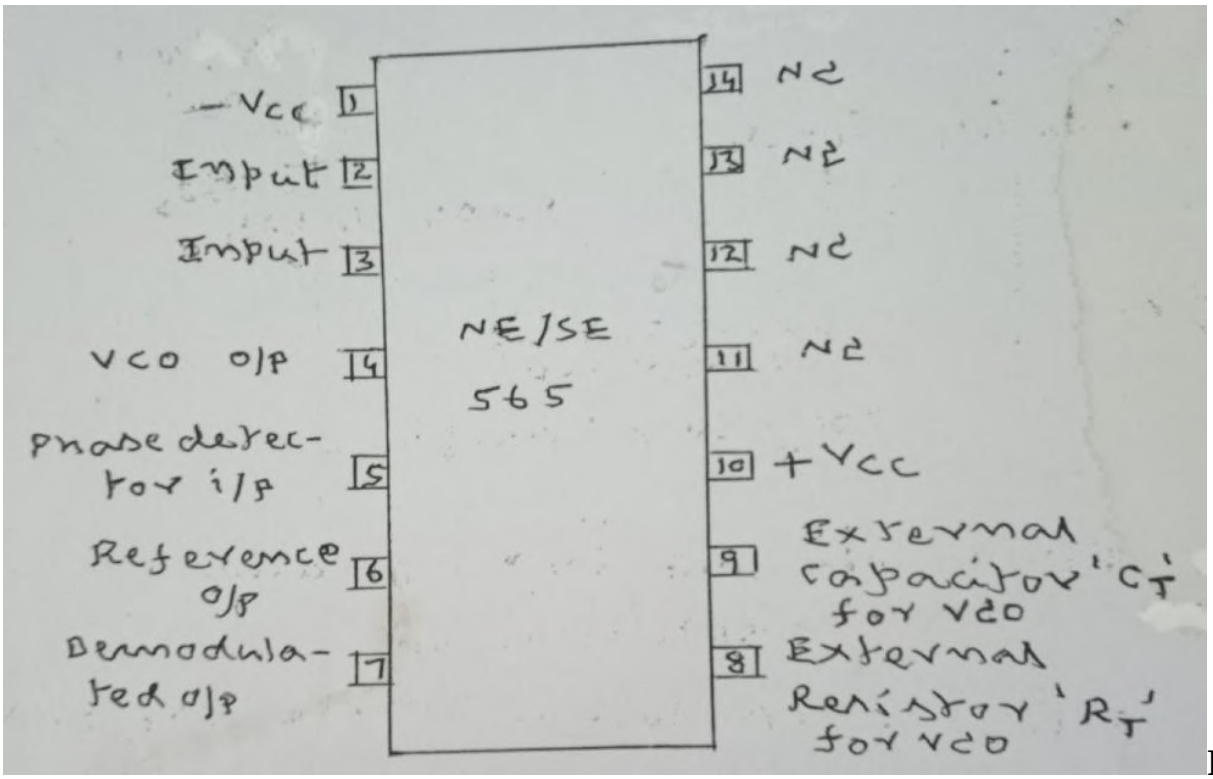


Fig. 11(a): Pin diagram of 565

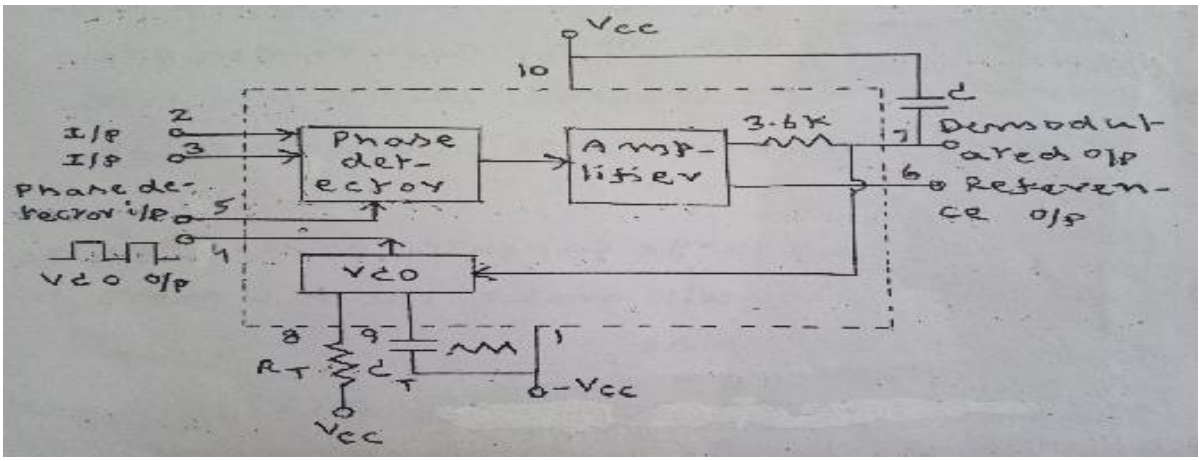


Fig. 11(b): Block diagram of 565

Fig. 11 (a) and Fig. 11 (b) represent the pin diagram and block diagram of 565. When inputs at pin 2 and pin 3 are grounded, VCO output is given by

$$f_o=\frac{0,25}{R_T C_T}\ \text{Hz}$$

Where R_T(2 KΩ to 20 KΩ)is external resistor connected to pin 8 and C_T is external capacitor connected to pin 9.

VCO free running frequency is adjusted by changing R_T or C_T and is kept at the center of i/p frequency range. PLL is 3.6 KΩ.

PLL is internally broken between VCO o/p and the phase comparator i/p. A short circuit between pins 4 and 5connects the VCO o/p to the phase comparator for comparing f_o and f_s. A Capacitor C is connected between pins 7 and 10 (Supply terminal) to make an LPF with the internal resistance of 3.6 KΩ

APPLICATIONS OF PLL

1. Frequency Translation
2. Frequency Multiplication/Division
3. AM Detection
4. FM Demodulator
5. FSK Demodulator

1.Frequency Translation (frequency shifting):

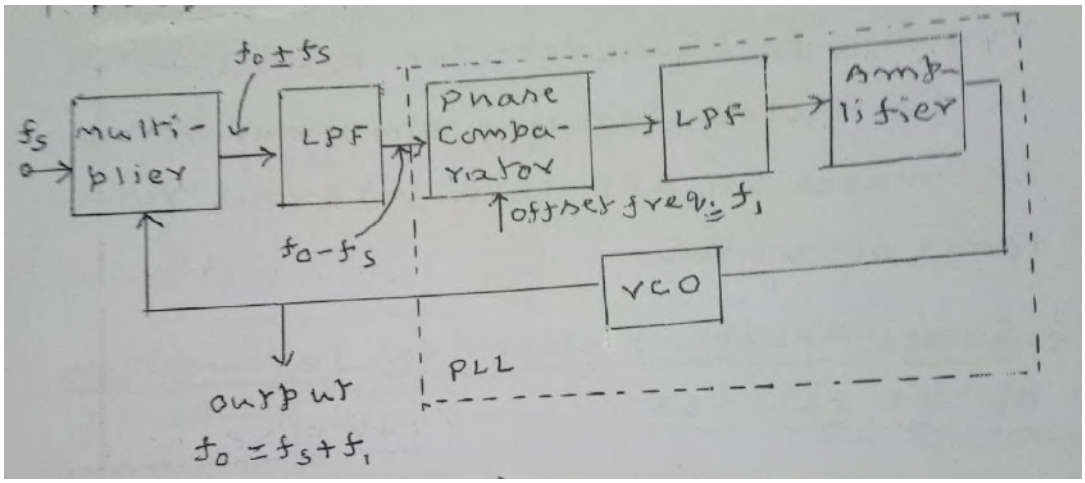


Fig. 12: Frequency translation using PLL

Here, a mixer (or multiplier) and an LPF are externally connected to PLL as shown in Fig. 12. Let f_s be the signal to be shifted in frequency (by an amount f_1).Let f_o is the o/p of VCO. Then f_s and f_o are the two inputs to the mixer (multiplier). Output of mixer contain $f_o \pm f_s$.

$f_o + f_s$ is rejected by LPF. So, LPF o/p contains $f_o - f_s$.

This $f_o - f_s$ is given as 1stinput to phase comparator. Offset (or translation) frequency f_1 is given as 2nd i/p to comparator. When PLL is in locked state,

$$f_o - f_s = f_1$$

i.e., $$\mathbf{f_o = f_s + f_1}$$

Thus, f_s is translated by an amount f_1.

2. Frequency Multiplication and Division:

(a) Frequency Multiplication by N:

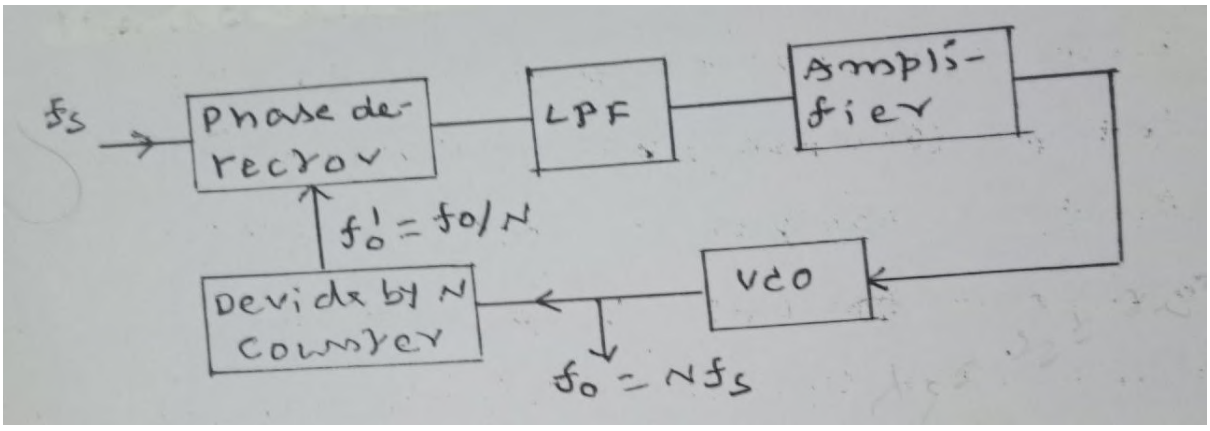


Fig. 13:Frequency Multiplier

Fig. 13shows the block diagram of a frequency multiplier. Here a ÷ N network (counter) is inserted between VCO and phase comparator. Let f_o' be the output. At locking,

$$f_s = f_o' = f_o/N$$

i.e., $$\mathbf{f_o = N f_s}$$

Thus, the circuit actsas a frequency multiplier.

(b) Frequency Division by M:

Here ÷ N network is not needed. If VCO is rich in harmonics, division is performed by locking M^{th} harmonic of VCO output to the input signal.

3. AM Detector:

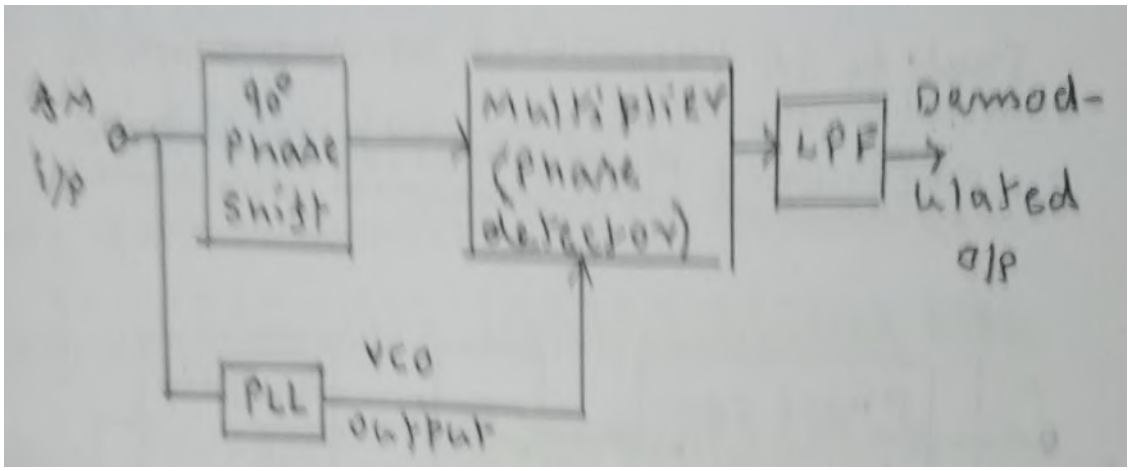


Fig. 14: AM Detector using PLL

Fig. 14 shows the block diagram of AM detector using PLL. Here PLL is locked to the carrier frequency of AM i/p. VCO o/p has same frequency of carrier. But it is 90^0 out of phase with AM signal. So, AM signal is shifted in phase by 90^0 before applying to multiplier. Thus, both inputs to multiplier are same in phase. Multiplier o/p consists of sum and difference terms. LPF allows only difference term. Output of LPF is demodulated o/p. This circuit has high selectivity and noise immunity.

4. FM demodulator:

Here PLL is locked to FM signal. VCO tracks the instantaneous frequency of the i/p signal. Output of LPF is demodulated o/p. It controls the VCO and maintains lock with the i/p signal.

5. FSK Demodulator:

In digital data communication, binary data is transmitted by means of a carrier frequency which is shifted between two pre-set values. This type of transmission is called Frequency Shift Keying (FSK). The binary data can be retrieved using an FSK demodulator using PLL.

Problem 3: Determine the dc control voltage v_c at lock, if the signal frequency f_s = 10 KHz, VCO free-running frequency is 10.66 KHz and the voltage to frequency transfer coefficient of VCO is 6600 Hz/Volt.

Solution:

We know that

$$\mathbf{f_s = f_0 + k_v v_c}$$

i,e., $v_c = \frac{f_s - f_o}{k_v}$

Given f_s = 10 KHz = 10000 Hz

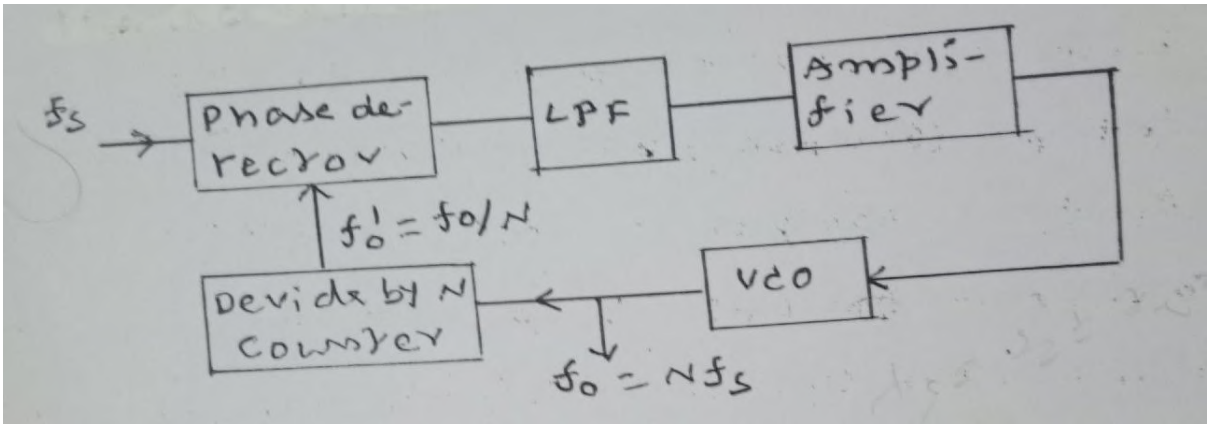
f_o = 10.66 KHz = 10660 Hz

And k_v = 6600 Hz/Volt

∴ DC control voltage $v_c = \frac{10000 - 10660}{6600}$ = - 0.1 V

Problem 4: For PLL, Determine the dc control voltage v_c at lock, if the signal frequency f_s = 100 KHz, VCO free running frequency is 5 MHz and the voltage to frequency transfer coefficient of VCO is 2 MHz/Volt and N = 100 in the frequency multiplier circuit given below. What is the dc voltage at lock?

Solution:



Given

f_s = 100 KHz

f_o = 5000 KHz

N = 100

∴ $f_o = \frac{5000\ KHz}{N} = \frac{5000\ KHz}{100}$ = 50 Hz

$$\mathbf{f_s = f_o' + k_v v_c}$$

i.e., $v_c = \frac{f_s - f_o'}{k_v}$

$= \frac{(100 - 50) \times 103}{2 \times 10^6} = 25$ mV

Problem 5: A PLL has a free running frequency of 500 KHz and bandwidth of low pass filter (LPF) is 10 KHz. Will the loop acquire lock for an input signal of 600 KHz? Justify your answer. Assume that phase detector produces an o/p of 50 mV dc.

Solution:

O/p of phase detector contains sum term $f_s + f_o$ and difference term $f_s - f_o$

Given f_s = 600 KHz and f_o = 500 KHZ

$f_s + f_o$ = 600 KHZ + 500 KHZ = 1100 KHz

$f_s - f_o$ = 600 KHZ – 500 KHZ = 100 KHz.

Hence both sum and difference terms are outside the pass band.

So, loop will not acquire lock, irrespective of v_c value given.

QUESTION BANK ON UNIT-3

Main Questions

1. What are different types of Electrical filters? Define and describe the frequency response of each type.

2. Describe a first order LPF/HPF and derive the necessary expression for its transfer function. Also derive an expression for the magnitude of the Transfer Function in dB.

3. (a) What is a band pass filter? Derive an expression for the transfer function

of a wide band pass filter.

(b) Problem on BPF.

4. What is an all pass filter (APF)? With the help of a diagram derive the necessary expressions for the magnitude of its o/p and phase anglebetween i/p and o/p. What is the main application of APF?

5. With the help of pin connection diagram and functional diagram explain the operation of a 555 timer in monostablemode. Derive an expression its output pulse width.

5. With the help of pin connection diagram and functional diagram explain the operation of a 555 timer in astable mode.Derive an expression for for its time period/frequency and duty cycle.

6. With the help of a block diagram, explain the principle of operation of PLL.

7. Describe 565 VCO used in PLL using Pin diagram and functional diagram.

8. Explain a monolithic IC (566 IC PLL)

9. Describe a second order LPF/HPF and derive the necessary expression for its transfer function. Also derive an expression for the magnitude of the Transfer Function in dB.

2 Marks Questions

1. Distinguish between analog active and passive filters.

2. What are the advantages of analog active filters over analog passive filters?

3. Draw the circuit of a first order wide BPF.

4. Draw the circuit of a wide BRF.

5. Draw the circuit of a notch filter.

6. What is an APF and what is its main application?

7. Draw the Circuit of a first order LPF.

8. Draw the Circuit of a first order HPF.

9. Draw the Circuit of a second order LPF.

10. Draw the Circuit of a second order HPF.

11. List the applications of a 555 timer in various areas.

12. Draw the block diagram of a PLL used for frequency translation.

13. Draw the block diagram of a PLL used for frequency multiplier.

14. What is the role of a phased detector in PLL?

15. What is the role of an LPF in PLL?

16. Define the terms lock-in range, capture range and pull-in time.

17. List the applications of a 555-timer used in monostable mode.

18. List the applications of a 555-timer used in astable mode.

19. What is the role of reset input in 555 timer?

20. What is the role of Pin 5 in a 555 timer?

Objective Questions

Objective Questions for I Mid:

31. Active filters used in phase correction in analog systems are ------ filters.
    (a) Low pass (b) High pass (c) Band pass **(d) All pass**
32. The roll off rate for 2nd order HPF is
    (a) - 30 dB / decade**(b) - 40 dB / decade** (c) - 20 dB / decade(d) - 10 dB / decade
33. The roll off rate for 2nd order LPF is
    (a) - 30 dB / decade**(b) - 40 dB / decade** (c) - 20 dB / decade(d) - 10 dB / decade
34. The magnitude of transfer function of fist order LPF is **Ans: (b)**
    (a) $\frac{A_o}{\sqrt{1+\left(\frac{f_l}{f}\right)^2}}$ **(b)** $\frac{\boldsymbol{A_o}}{\sqrt{\mathbf{1}+\left(\frac{\boldsymbol{f}}{\boldsymbol{f_h}}\right)^{\mathbf{2}}}}$ (c) $\frac{A_o}{\sqrt{1+\left(\frac{f_l}{f}\right)^4}}$ (d) $\frac{A_o}{\sqrt{1+\left(\frac{f}{f_h}\right)^4}}$
35. The magnitude of transfer function of fist order HPF is **Ans:(a)**
    (a) $\frac{\boldsymbol{A_o}}{\sqrt{\mathbf{1}+\left(\frac{\boldsymbol{f_l}}{\boldsymbol{f}}\right)^{\mathbf{2}}}}$ (b) $\frac{A_o}{\sqrt{1+\left(\frac{f}{f_h}\right)^2}}$ (c) $\frac{A_o}{\sqrt{1+\left(\frac{f_l}{f}\right)^4}}$ (d) $\frac{A_o}{\sqrt{1+\left(\frac{f}{f_h}\right)^4}}$
36. The magnitude of transfer function of Second order LPF is **Ans:(d)**
    (a) $\frac{A_o}{\sqrt{1+\left(\frac{f_l}{f}\right)^2}}$ (b) $\frac{A_o}{\sqrt{1+\left(\frac{f}{f_h}\right)^2}}$ (c) $\frac{A_o}{\sqrt{1+\left(\frac{f_l}{f}\right)^4}}$ **(d)** $\frac{\boldsymbol{A_o}}{\sqrt{\mathbf{1}+\left(\frac{\boldsymbol{f}}{\boldsymbol{f_h}}\right)^{\mathbf{4}}}}$
37. The magnitude of transfer function of second order HPF is **Ans:(c)**
    (a) $\frac{A_o}{\sqrt{1+\left(\frac{f_l}{f}\right)^2}}$ (b) $\frac{A_o}{\sqrt{1+\left(\frac{f}{f_h}\right)^2}}$ **(c)** $\frac{\boldsymbol{A_o}}{\sqrt{\mathbf{1}+\left(\frac{\boldsymbol{f_l}}{\boldsymbol{f}}\right)^{\mathbf{4}}}}$ (d) $\frac{A_o}{\sqrt{1+\left(\frac{f}{f_h}\right)^4}}$
38. The damping factor of a Butterworth filter is
    (a) 1.06(b) 1.73 **(c) 1.44**(d) .707
39. First order BPF is a cascade of first order------- followed by first order ------ respectively.
    (a) HPF, LPF (b) LPF, LPF (c) HPF, HPF (d) LPF, HPF
40. Expression for the f_o of BPF is --------
    (a) $f_h + f_l$ (b) $f_h f_l$ **(c)** $\sqrt{\boldsymbol{f_h f_l}}$ (d) $f_h - f_l$

Objective Questions for II Mid

41. Modulating voltage is applied at ----- of a 555 timer
    (a) 3 (b) 4**(c) 5**(d) 7
42. Pulse width of a monostable multivibrator using PLL is -------
    (a) 1.1 RC (b) 0.69 RC (c) RC ln (0.69)(d) RC ln 1.1
43. 555 timer in astable multivibrator mode is used for -------

(a) Pulse width modulation (PWM) (b) **Pulse position modulation (PPM)** (c) Both(d) None

44. If $R_A = R_B$, duty cycle of a 555 timer astable multivibrator is -------
(a) 0% **(b) 50%** (c) 75%(d) 100%

45. Formula for the time period dof a 555 timer astable multivibrator is ------
(a) 0.69 (R_A + R_B) C **(b)0.69 (R_A + 2 R_B) C**
(c) $\frac{1}{(0.69\ (R_A\ +2\ R_B)\ C}$)C(d)$\frac{1}{(0.69\ (R_A\ +\ R_B)\ C}$

46. LPF in a PLL allows ------- frequency term.
(a) Difference term (b) Sum term (c) Both terms(d) None

47. Range of frequencies over which a PLL can acquire a lock is called ------
(a) Pull-in time (b) Lock-in range (c) Maintain range **(d) Capture range**

48. NE/SE 565 is a ----------.
(a) IC VCO (b) IC Phase detector **(c) IC PLL** (d) IC LPF

49. NE/SE 566 is a ----------.
(a) IC VCO (b) IC Phase detector(c) IC PLL(d) IC LPF

50. Which of the following is correct in case of PLL ----------.
(a) Capture range > Lock-in range **(b)Lock-in range > Capture range**
(c) Capture range = Lock-in range (d) we can't say anything

UNIT-4

VOLTAGE REGULATORS AND CONVERTERS

D TO A & A TO D CONVERTERS

Some electronic systems operate on only digital signals. If analog signals are available, we need to convert them to digital form. This can be done by a circuit called Analog to Digital ('A to D' or A/D) converter or ADC.

Similarly, some electronic systems operate with only analog signals. If digital signals are available, we need to convert them to analog form. This can be done by a circuit called Digital to Analog ('D to A' or D/A) converter or DAC.

DIGITAL TO ANALOG CONVERTERS (DACs)

A DAC is a circuit which converts digital signals into analog form.

Basic DAC Technique:

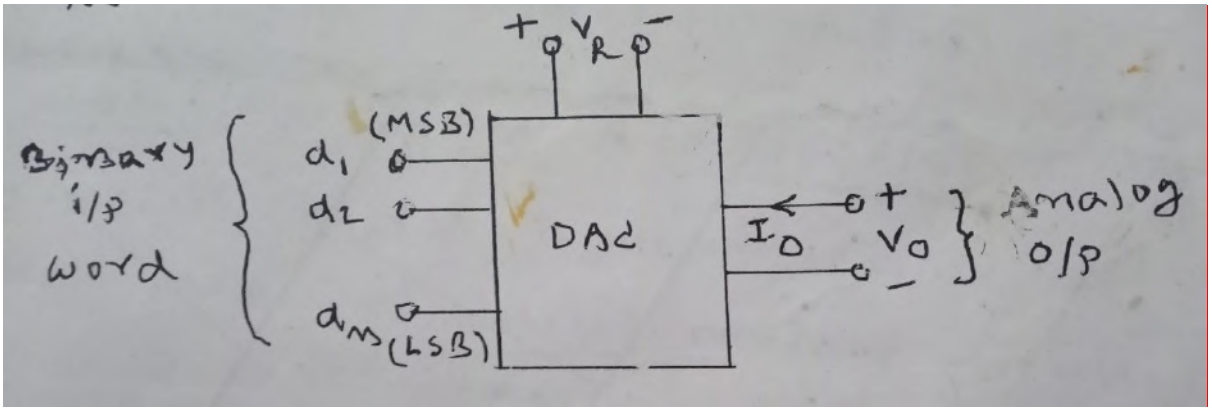


Fig. 1: Schematic diagram of a DAC

Fig. 1 shows the schematic diagram of an n-bit DAC. Its i/p is an n-bit binary word. It is combined with a reference voltage V_R to produce an analog o/p signal. It may be voltage or current. If o/p is voltage, it is given by

$v_o = K V_{FS} (d_1 2^{-1} + 2^{-2} + \ldots\ldots\ldots\ldots d_n 2^{-n})$

Where

v_o = o/p voltage

V_{FS} = Full scale o/p voltage

K = Scaling factor (usually K = 1)

$d_1 d_2 \ldots d_n$= n–bit binary fractional word with decimal point at the left.

d_1 = MSB with a weight of $\frac{V_{FS}}{2}$

d_n = LSB with a weight of $\frac{V_{FS}}{2^n}$

Types of DACs:

1. Binary weighted resistor type DAC
2. r- ladder type DAC
3. Inverted R-2R ladder type DAC

1. BINARY WEIGHTED RESISTOR TYPE DAC

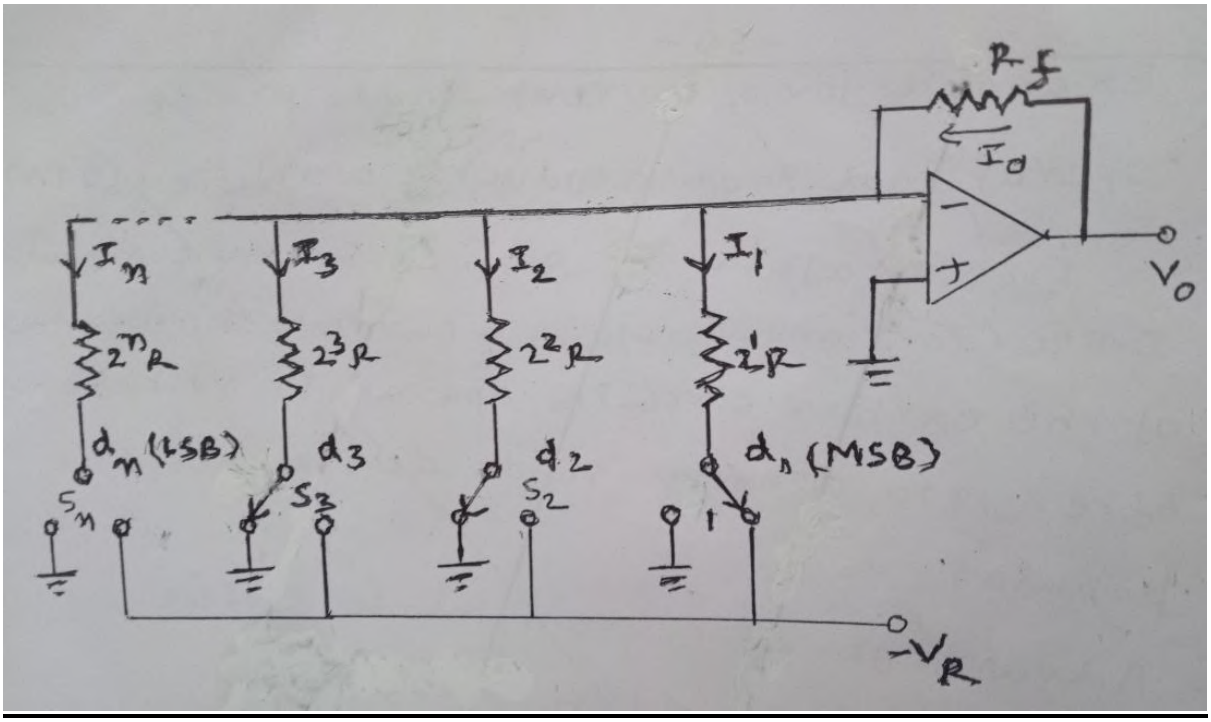


Fig. 2 (a): Binary weighted resistor type DAC

Fig. 2 (a) shows a binary weighted resistor type DAC. Here opamp is in inverting mode. We can also use non-inverting mode.

Opamp is a summing amplifier. It acts as a current-to-voltage converter.

S1, S2, … Sn are MOSFET switches used as Single pole double throw (SPDT) switches.

Upper end of any switch is connected to – ve terminal of opamp. Lower end of any switch S_i (i = 1, 2, … n) has two positions. In left position, S_i is grounded. In right position, it connects a resistor 2^i R to reference voltage – V_R. Polarity of V_R may be + ve or – ve. Here V_R is taken – ve.

From Fig. 2(a), we write

$$I_0 = I_1 + I_2 + \ldots + I_n$$

$$= \frac{V_R}{2^1 R} d_1 + \frac{V_R}{2^2 R} d_2 + \ldots + \frac{V_R}{2^n R} d_n$$

$$= \frac{V_R}{R} \{d_1 2^{-1} + d_2 2^{-2} + \ldots + d_n 2^{-n}\}$$

$\therefore v_o = I_o R_f = V_R \frac{R_f}{R} \{d_1 2^{-1} + d_2 2^{-2} + \ldots + d_n 2^{-n}\}$ …(1)

But general equation of a DAC is

$v_o = K V_{FS} (d_1 2^{-1} + 2^{-2} + \ldots\ldots\ldots\ldots d_n 2^{-n})$ … (2)

Comparing eqs. (1) and (2). We get

$R_f = R$ $K = 1$ and $V_{FS} = V_R$

Accuracy and stability of this DAC depends on the accuracy and temperature tracking of resistors.

Fig. 2(b) show the transfer characteristics of a 3-bit weighted resistor DAC. It is a staircase waveform. The inclined dashed line passesthrough averages of o/p value in each step.

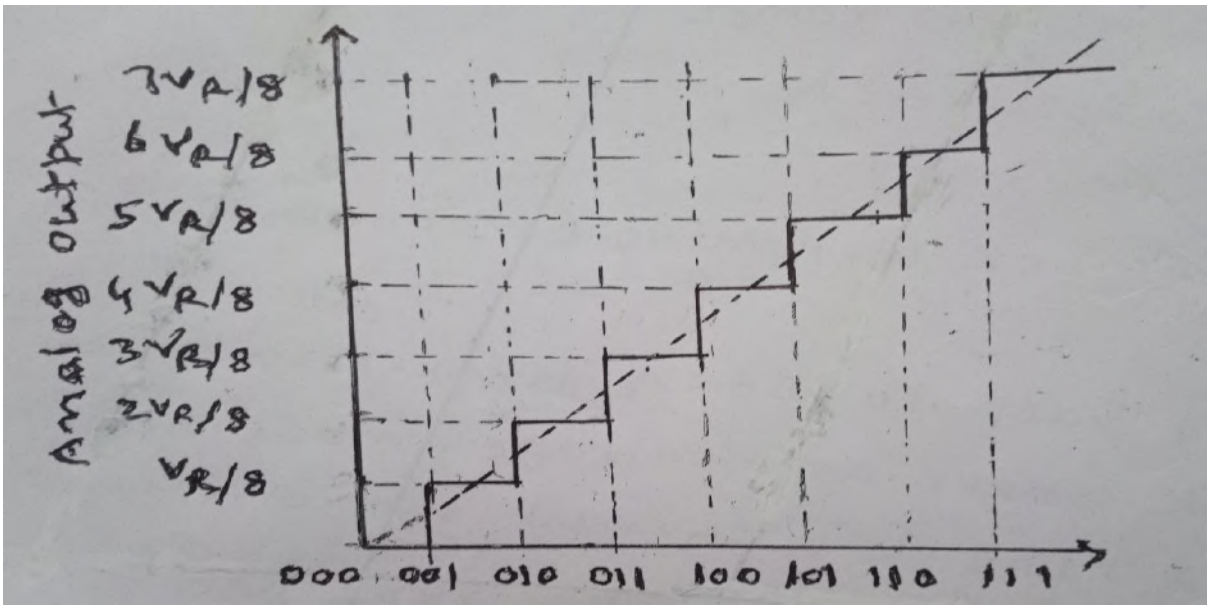


Fig. 2 (b) Waveform for binary weighted DAC

Problem with this DAC:

It needs wide range of resistor values. We use large number of bits to increase the resolution. This increases the range of resistor values.

Example:

If smallest resistor is 2.5 KΩ, largest one is 5.2 MΩ. Such large resistance cannot be fabricated in IC form. Also, voltage drop acrossit affects the accuracy.

If smallest resistor is < 2.5 KΩ, it causes loading effect.

So, this type of DAC is very difficult to fabricate in IC form.

2. R-2R LADDER TYPE DAC

Wide range of resistors are required in binary weighted resistor DAC. This problem can be avoided by using R–2R ladder DAC, where only two resistor values are required.

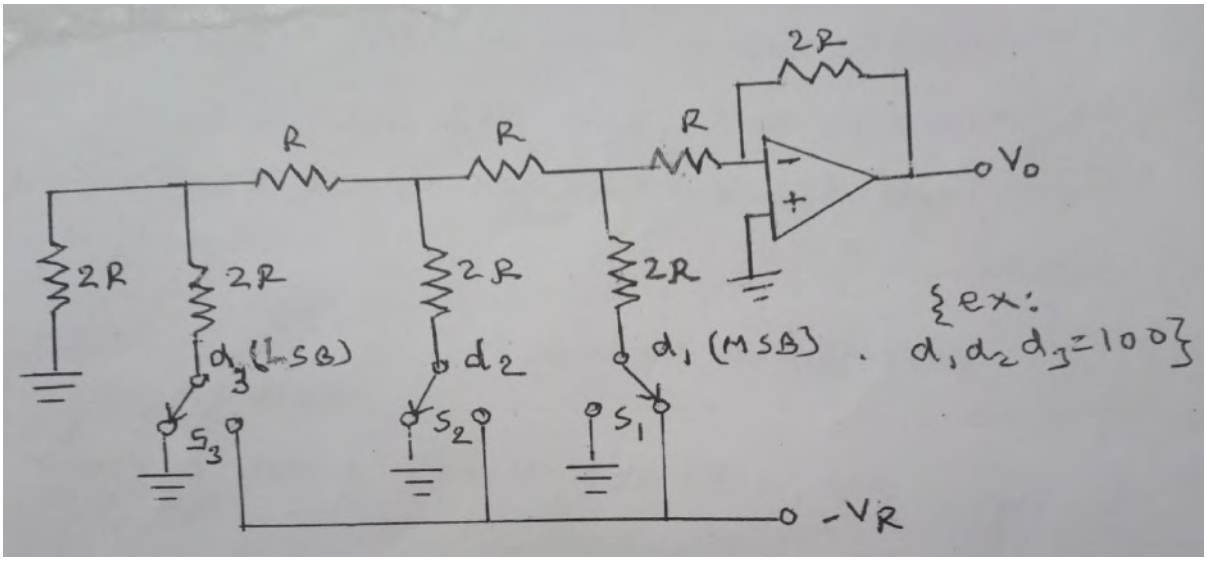
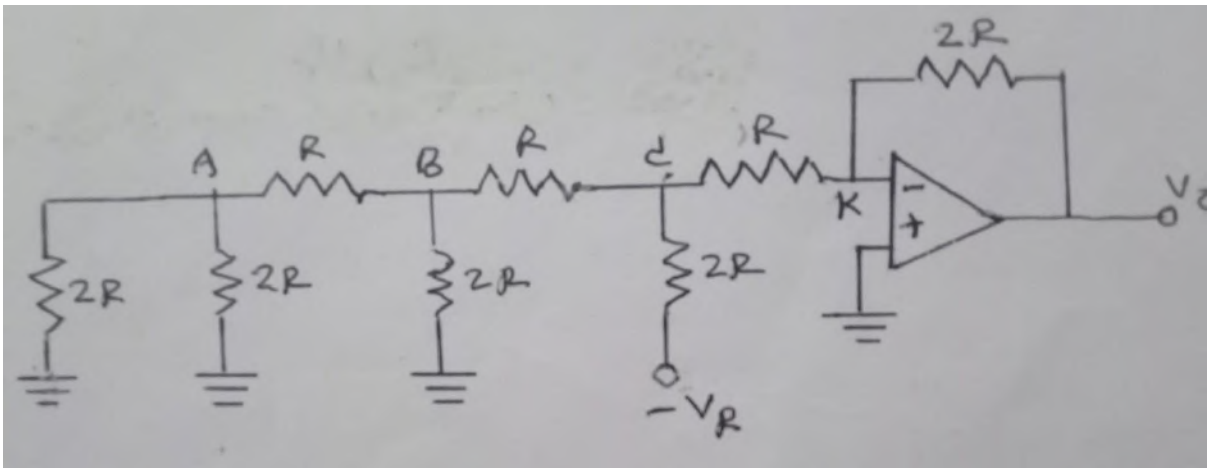


Fig. 3 (a): R-2R ladder type DAC

Fig. 3 (a) shows a 3-bit R-2R ladder DAC. Its binary input word is d_1 d_2 d_3, where d_1 = and d_3 = LSB. S_1, S_2 and S_3 are 3 MOSFET switches used as Single pole double throw (SPDT) switches.

Upper end of each switch is connected to – ve terminal of opamp. Lower end of any switch S_i (i = 1, 2, 3) has two positions. In left position, S_i is grounded. In right position, it connects a resistor 2R to reference voltage – V_R. Polarity of V_R may be + ve or – ve. Here V_R is taken – ve.



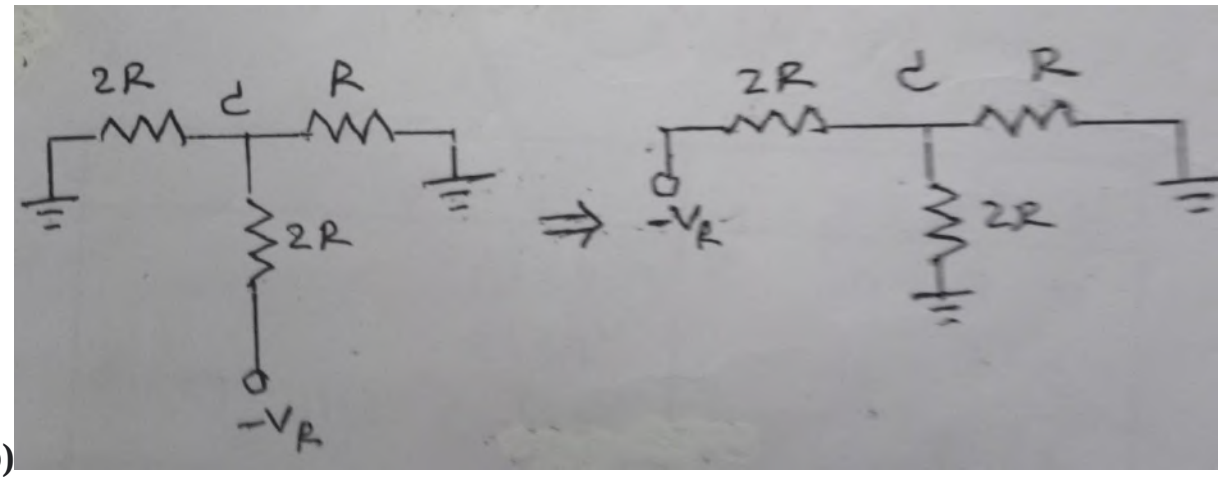


Fig. 3 (b)

Fig. 3 (c)

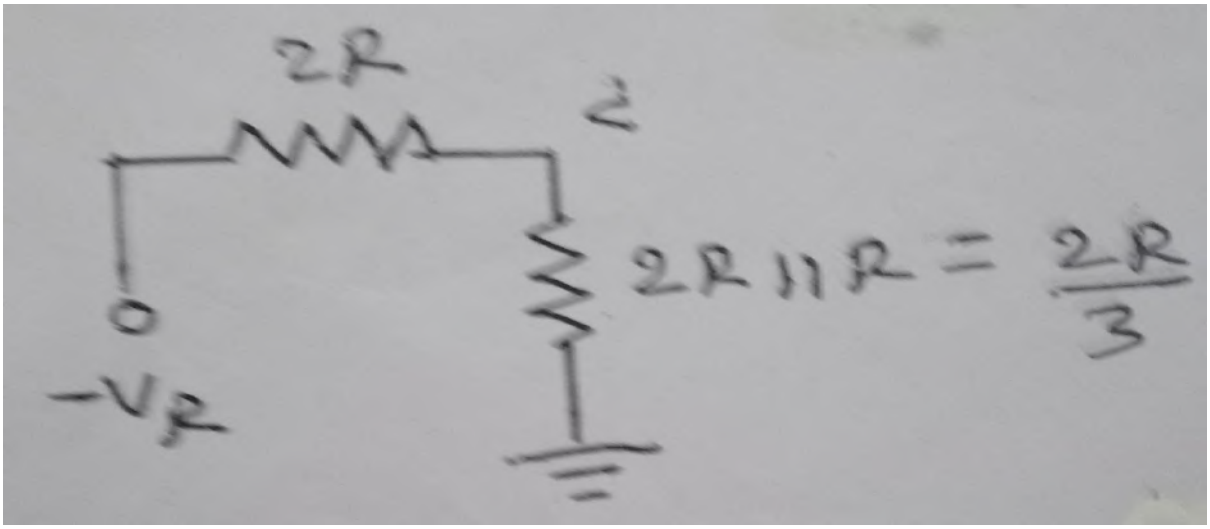


Fig. 3 (d)

Fig. 3 (b) shows equivalent circuit for Fig. 3 (a), where $d_1\ d_2\ d_3 = 100$.

Using network analysis, Fig. 3 (b) reduces to Fig. 3 (c) and then Fig. 3 (d).

Voltage at node C = $-V_R \cdot \frac{\frac{2R}{3}}{2R+\frac{2R}{3}} = -V_R \cdot \frac{2R}{8R} = -\frac{V_R}{4}$

Then Fig. 3 (e) represents the final circuit.

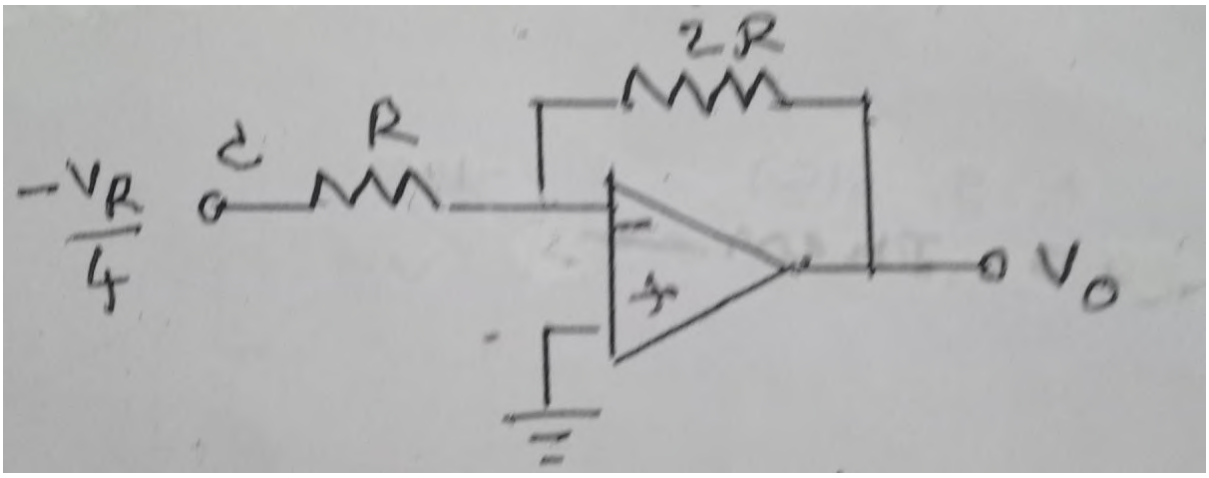


Fig. 3 (e) Final equivalent circuit

From Fig. 3 (e), we get

$$v_o = -\frac{V_R}{4}\left(\frac{-2R}{R}\right) = \frac{V_R}{2} = \frac{V_{FS}}{2}$$

Similarly, we can find v_o for any value of d_1 d_2 d_3.

3. INVERTED R–2R LADDER TYPE DAC

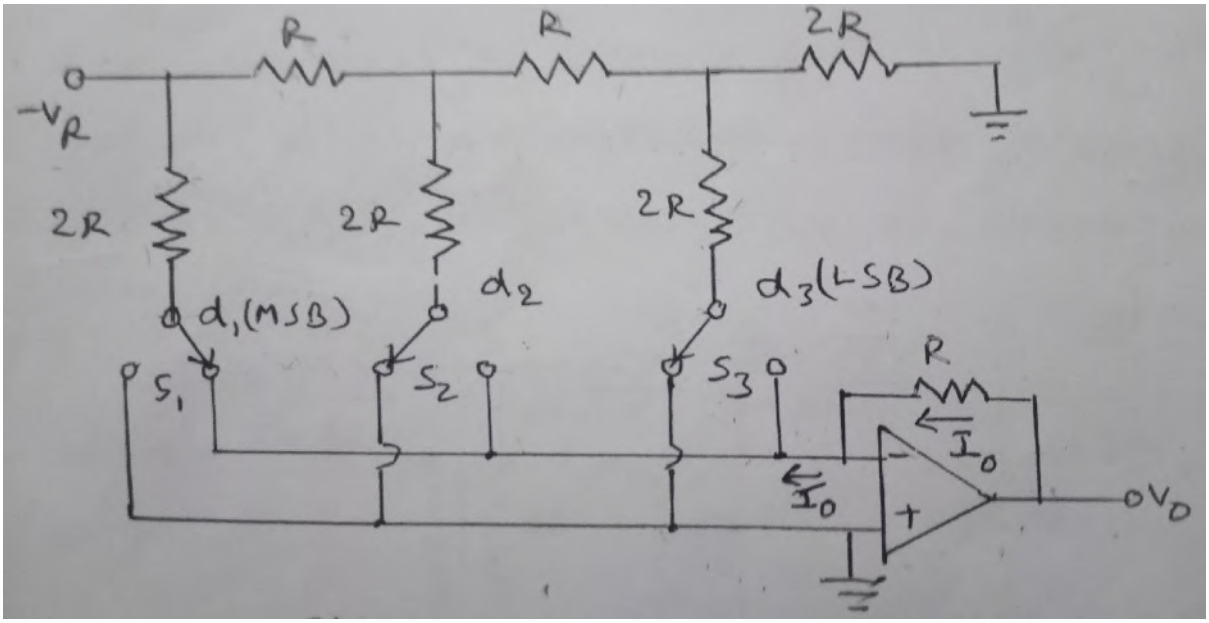


Fig. 4(a): 3-bit Inverted ladder DAC

Fig. 4(a) shows a 3-bit Inverted ladder DAC. Compared to ladder DAC, positions of MSB and LSB are interchanged.

S_1, S_2 and S_3 are 3 MOSFET switches of SPDT type. In left position, S_i is grounded. In right position, any switch is connected to the – ve terminal of an ideal opamp, which acts as a

virtual ground. Since both terminals of any switch are at ground potential, current flowing in any resistor branch is constant and independent of switch position (i.e., input binary word).

Important property of this circuit is that current divides equally at each node. It is because equivalent resistance to the left of any node or right of any node is 2R.

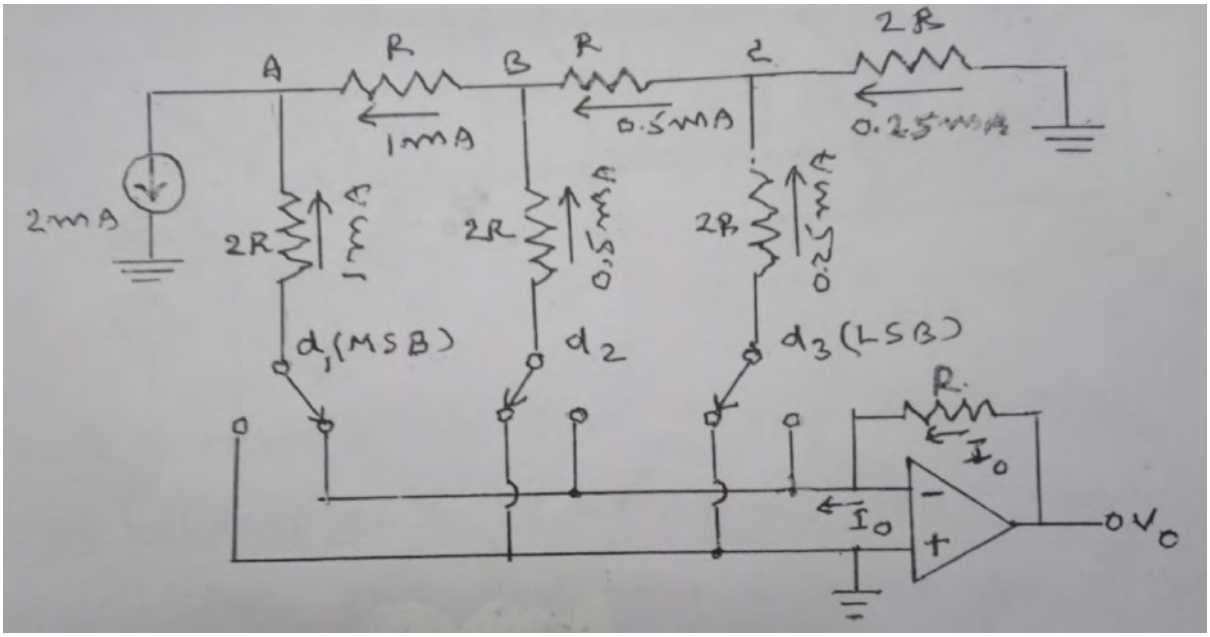


Fig. 4 (b) Illustrative example with 2 mA current

Fig. 4 (b) illustrates the division of a 2 mA current at each node. For example, current divides equally as 1 mA to the left and right of node A.

Current remains constant in any resistive branch. So, nodal voltages remain constant at $\frac{V_R}{2^0}$, $\frac{V_R}{2^1}$and $\frac{V_R}{2^2}$. But current I_o in feedback resistor depends on input binary word.

The circuit works on the principle of summing currents and operates in current mode.

Problem 4.1: The basic step of an 8-bit DAC is 10.2 mV. If 00000000 represents 0 Volts, what is the o/p produced if the i/p is 10010111?

Solution:

The o/p produced for input 10010111

$= 10.2 \text{ mV } (1 \times 2^7 + 0 \times 2^6 + 0 \times 2^5 + 1 \times 2^4 + 0x\ 2^3 + 1 \times 2^2 + 1 \times 2^1 + 1 \times 2^0)$

$= 10.2 \text{ mV} \times 151 = 1.54 \text{ V}$

Problem 4.2: Calculate the values of LSB, MSB and full-scale output for an 8–bit DAC for 0 to 10 V range.

Solution:

LSB = $\frac{V_{FS}}{2^n}$ and MSB = $\frac{V_{FS}}{2}$

Given that V_{FS} = 10 V and n = 8

∴ LSB = $\frac{10\ V}{256}$ = .039 V = 39 mV

MSB = $\frac{10\ V}{2}$ = 5 V

Full scale o/p = V_{FS} – 1 LSB

= 10 V – 0.039 V

= 9.961 V

Problem 4.3: What o/p voltage would be produced by a 4-bit DAC whose o/p range is 0 to 10 V, for a digital input 0110?

Solution:

Output voltage = V_{FS} ($d_1\ 2^{-1} + d_2 2^{-2} + d_3 2^{-3} + d_4 2^{-4}$)

Given that V_{FS} = 10 V and $d_1\ d_2\ d_3\ d_4$ = 0110

∴Output voltage = 10 V (0 x $\frac{1}{2}$+ 1 x $\frac{1}{4}$ + 1 x $\frac{1}{8}$ + 0 x $\frac{1}{16}$)

= $\frac{30}{8}$ V = 3.75 V

ANALOG TO DIGITAL CONVERTERS (DACs)

An ADC is a circuit which converts analog signals into digital form.

Basic ADC Technique:

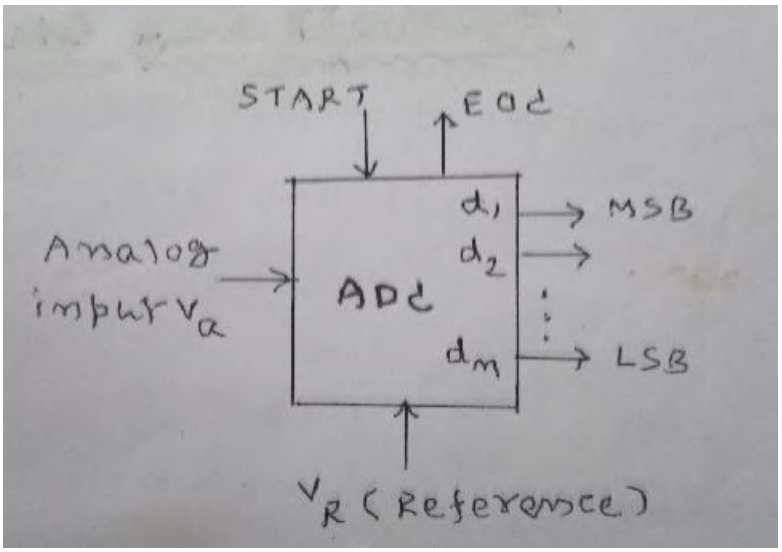


Fig. 5: Schematic diagram of an n-bit ADC

Fig. 5 shows the schematic diagram of an n-bit ADC. V_a its analog input voltage. Its digital o/p is d_1 d_2 ... d_n, where d_1 = MSB and d_n = LSB.

Functional value of **output = D = $d_1 2^{-1} + 2^{-2} + \ldots\ldots\ldots\ d_n 2^{-n}$**

ADC has 2 additional control lines START and EOC. START input indicates beginning of conversion, EOC (End of conversion) output indicates end of data conversion.

Applications of ADCs:

(i) Microprocessor interfacing
(ii) To directly drive LCD and LED displays
(iii) Digital voltmeters

Classification of ADCs:

ADCs are mainly classified as Direct type ADCs and Integrating type ADCs.

Direct type ADCs compare a given analog signal with internally generated equivalent signal.

Direct type ADCs:

1. Flash type ADC
2. Counter type ADC
3. Servo tracking ADC
4. Successive approximation type ADC

Integrating type ADCs(Indirect type ADCs) perform conversion in an indirect manner. They first convert the analog signal to a linear function of time (or frequency) and then to a digital code

Integrating type ADCS:

1. Single slope ADC
2. Dual slope ADC

Direct Type ADCs:

1. FLASH TYPE ADC (PARALLEL COMPARATOR TYPE ADC)

It is the simplest, **fastest** and costly ADC.

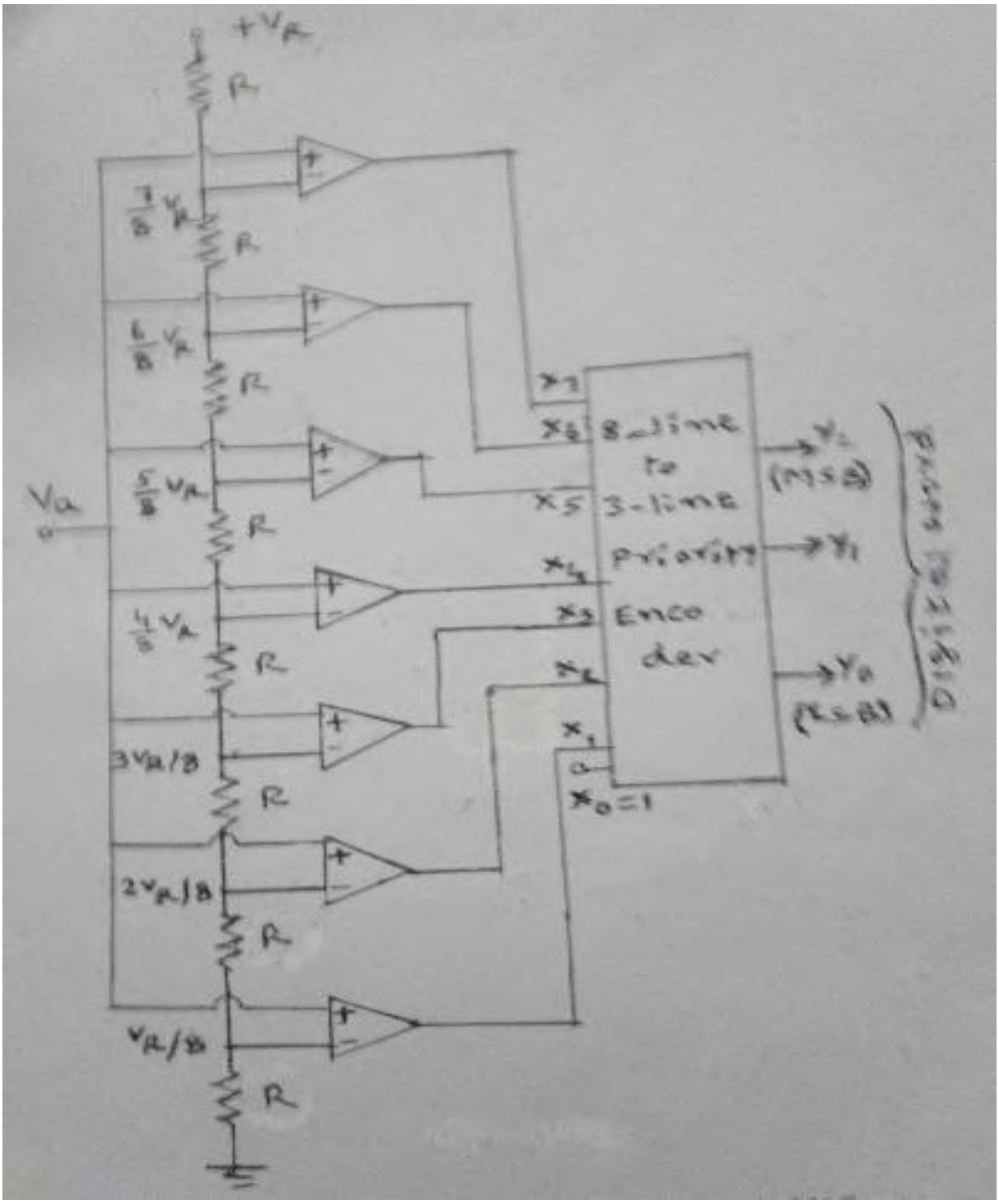


Fig. 6 (a):3–bit flash ADC

Fig. 6 (a) shows the circuit of a 3-bit flash ADC. It consists of a voltage divider, 7 comparators and an 8-line to 3-line priority encoder. Analog voltage V_a is applied to the + ve terminal of opamp comparators, X_1, X_2, … X_7 are the outputs of the comparators as shown. X_0, X_1, … X_7 are the inputs to priority encoder, where $X_0 = 1$. $Y_2Y_1Y_0$ is the binary output word where Y_2 = MSB and Y_0 = LSB.

8 resistors form a voltage divider between reference voltage V_R and ground. Let v_d be the input, fed to – ve terminal of opamps, where v_d changes from $\frac{V_R}{8}$ to $\frac{7\,V_R}{8}$ as shown.

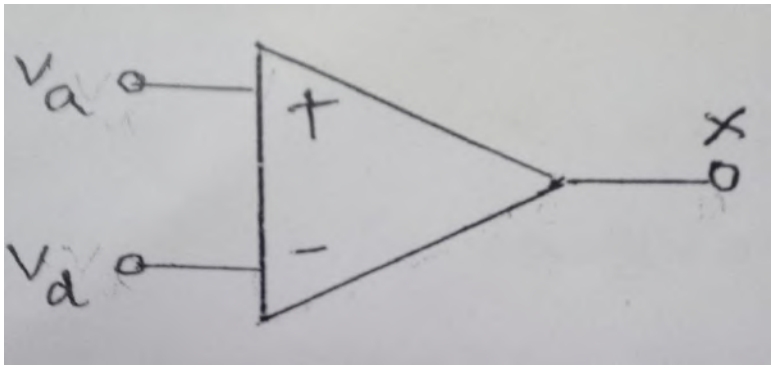


Fig. 6 (b) Comparator

Voltage input	Logic output X
$v_a > v_d$	X = 1
$v_a < v_d$	X = 0
$v_a = v_d$	Previous value

Fig. 6 (c) Comparator truth table

Input voltage v_a	**X7**	**X6**	**X5**	**X4**	**X3**	**X2**	**X1**	**X0**	**Y2**	**Y1**	**Y0**
0 to $\frac{5\,V_R}{8}$	0	0	0	0	0	0	0	1	0	0	0
$\frac{V_R}{8}$ to $\frac{2\,V_R}{8}$	0	0	0	0	0	0	1	1	0	0	1
$\frac{2\,V_R}{8}$ to $\frac{3\,V_R}{8}$	0	0	0	0	0	1	1	1	0	1	0
$\frac{3\,V_R}{8}$ to $\frac{4\,V_R}{8}$	0	0	0	0	1	1	1	1	0	1	1
$\frac{4\,V_R}{8}$ to $\frac{5\,V_R}{8}$	0	0	0	1	1	1	1	1	1	0	0
$\frac{5\,V_R}{8}$ to $\frac{6\,V_R}{8}$	0	0	1	1	1	1	1	1	1	0	1
$\frac{6\,V_R}{8}$ to $\frac{7\,V_R}{8}$	0	1	1	1	1	1	1	1	1	1	0
$\frac{7\,V_R}{8}$ to $\frac{8\,V_R}{8}$	1	1	1	1	1	1	1	1	1	1	1

Fig. 6 (d) Truth table for flash ADC

Fig. 6 (b) shows any comparator circuit. Fig. 6 (c) shows truth table of comparator. Fig. 6 (d) shows the truth table for the flash ADC. The circuit compares v_a with each nodal voltage.

Here conversion takes place in parallel (simultaneously) rather than sequentially. Conversion time is limited by speed of comparators and speed of priority encoder.

Drawback of the flash ADC:

An n-bit flash ADC requires 2^n – 1comparators where n is the number of bits in binary o/p word. i.e., number of comparators approximately doubles for each added bit. Also, the larger the value of n, the more complex is the priority encoder.

SUCCESSIVE APPROXIMATION TYPE ADC

It uses successive approximation technique and converts analog voltage to digital form.

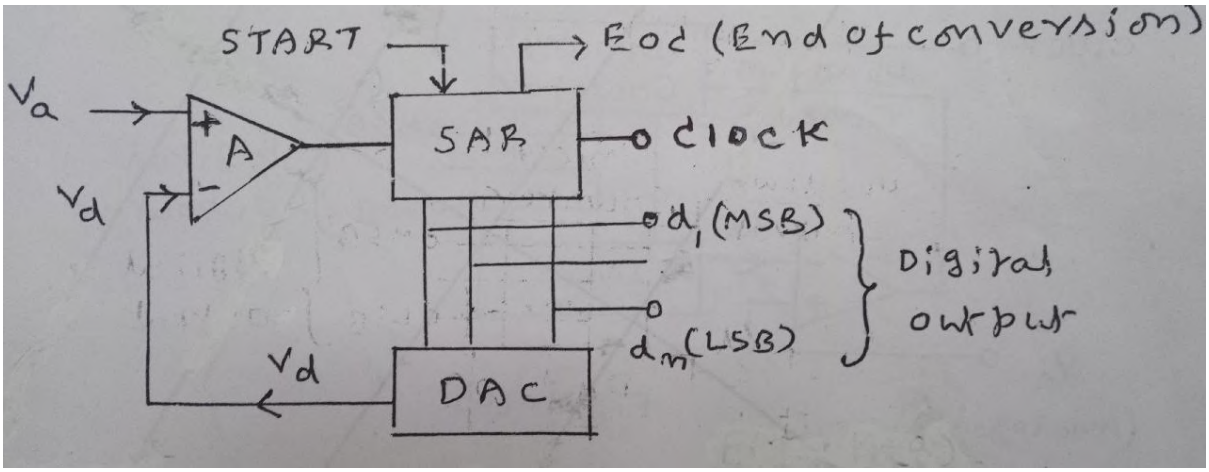


Fig. 7 (a)

Fig. 7 (a) shows the block diagram of an 8-bit successive approximation ADC. SAR stands for successive approximation register. Opamp 'A' is used as a comparator. V_a is the analog voltage to be converted to digital form. V_d is the analog o/p voltage of DAC. Output of SAR is a digital word $d_1d_2 \ldots d_n$. where d_1 = MSB and d_8 = LSB.

This 8-bit ADC requires 8 clock pulses for conversion process. An extra (9^{th}) pulse is used to load the output register and reinitialize the circuit.

SAR finds required value of each bit in digital o/p by trial and error.

When SAR receives START command, it sets MSB to '1' and other bits to zero. So, trial word is 10000000.

Comparator compares v_a and v_d.

If $v_d < v_a$, trial word is < correct word. Then MSB is left at 1 and next (2^{nd}) MSB is set to 1.

If $v_d > v_a$, trial word is > correct word. Then MSB is set to 0 and next (2^{nd}) MSB is set to 1.

The procedure is repeated for all bits (from MSB to LSB). Whenever $v_d > v_a$, the comparator changes its state.

For simplicity's sake, let us consider a 4-bit ADC as an example.

Then, Fig. 7 (b) indicates the conversion sequencefor a typical analog input.

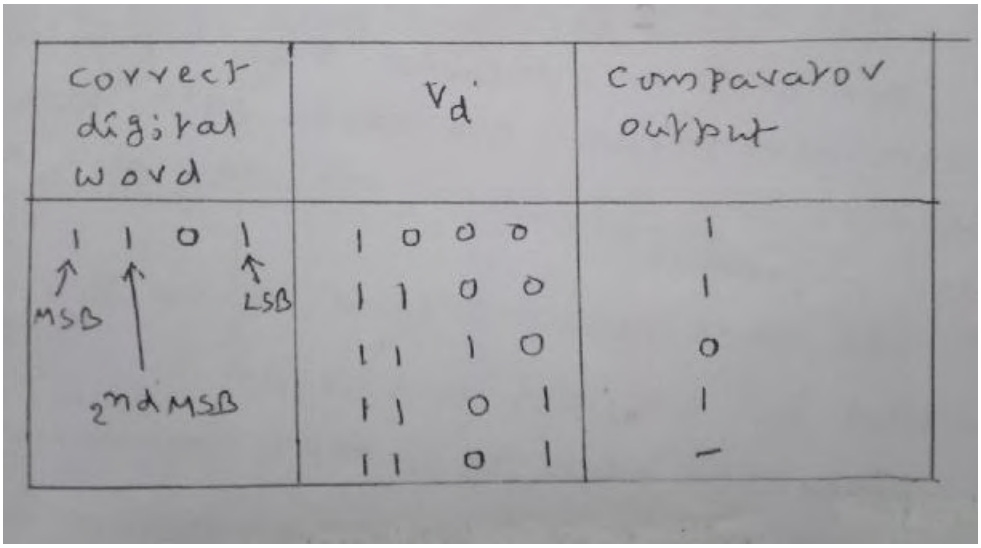


Fig. 7 (b):Conversion sequence

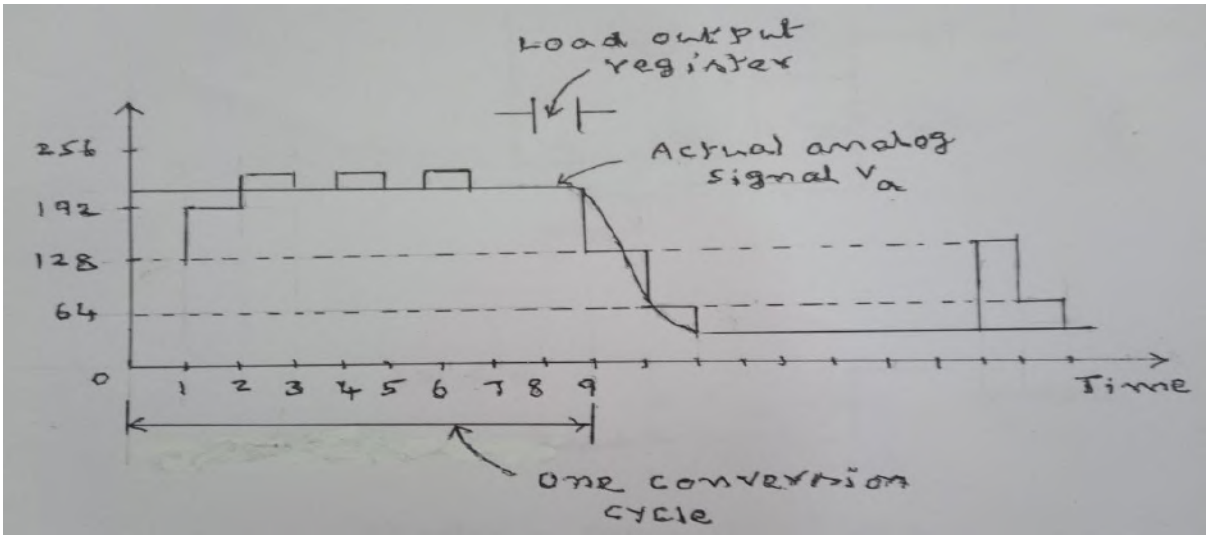


Fig. 7 (c): DAC output waveform

Fig. 7 (c) shows DAC o/p voltage waveform. Here the o/p voltage becomes successively closer to the actual analog i/p voltage.

DUAL SLOPE ADC (DUAL RAMP ADC)

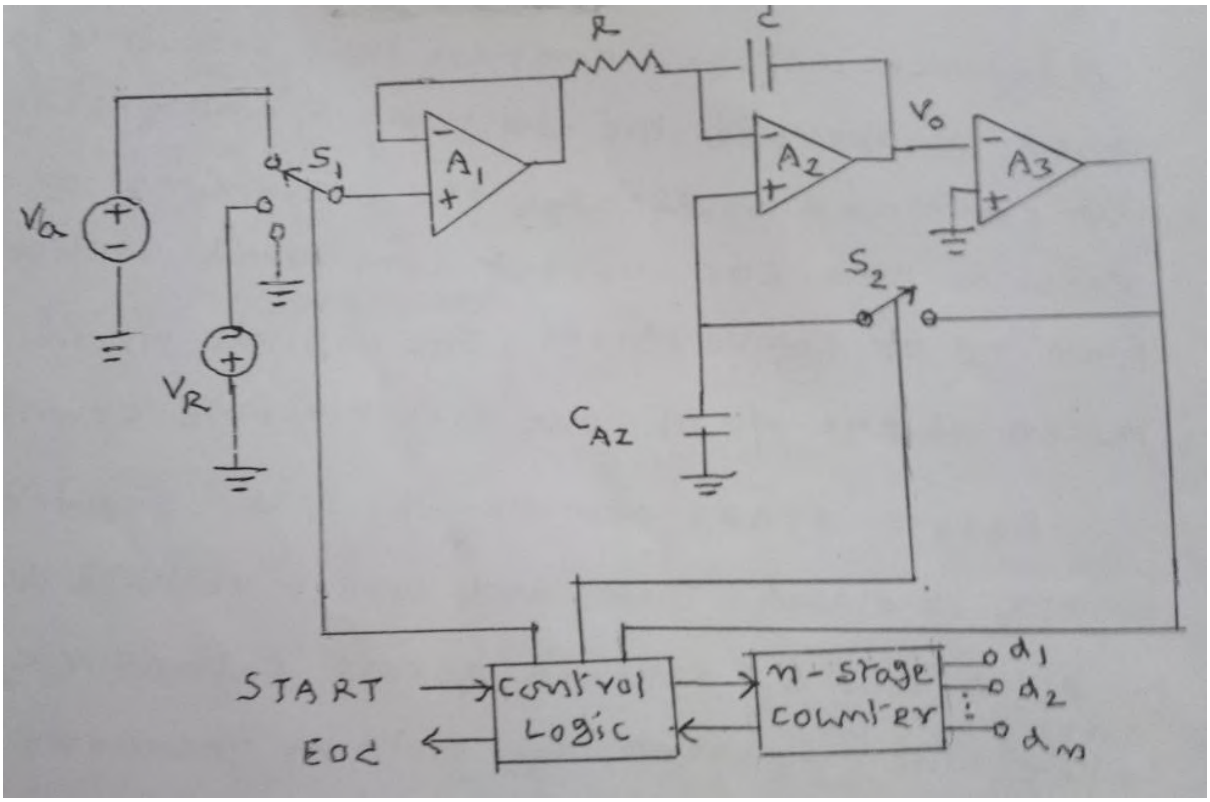


Fig. 8 (a): Functional diagram of dual slope ADC.

Fig. 8 (a) shows functional diagram of dual slope ADC. Opamps A_1, A_2 and A_3 act as buffer, integrator and comparator respectively.v_a is analog i/p voltage. – V_R is an internal reference voltage. Control logic circuitry is used to operate the switches S_1 and S_2. START input command indicates the beginning of conversion and EOC output command indicates the ending of conversion. The digital o/p is taken at the o/p of the n-bit ripple counter.

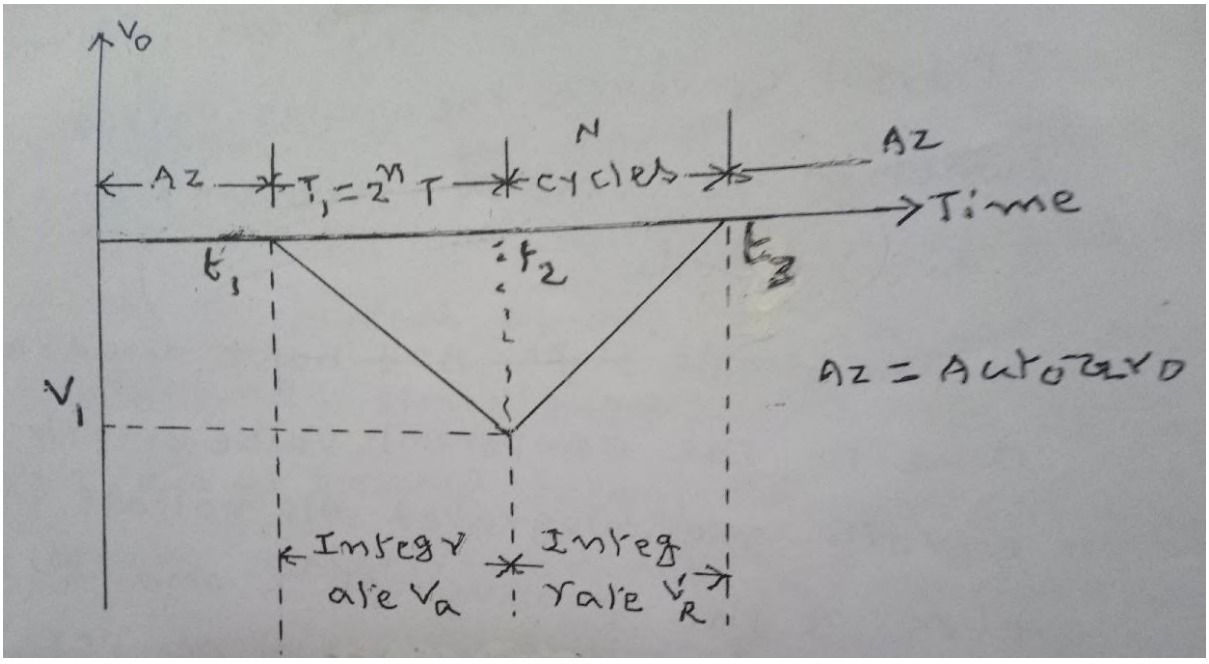


Fig. 8 (b) Output waveform for dual slope ADC

Fig. 8 (b) shows the o/p waveform for dual slope ADC. Before start command, S_1 is grounded and S_2 is closed. Then any offset voltage due to A_1, A_2 and A_3 appears across capacitor C_{AZ} (AZ means auto zero). Later, when S_2 opens, C_{AZ} acts as memory and holds i/p offset compensating voltage.

Let START command is given at $t = t_1$. Then control logic opens S_2 and connects $S_1$to v_a. It also enables counter start from zero count. The counter resets after 2^n clock pulses, say at $t = t_2$. Let T be the clock period. Then time of integration T_1 for $v_a$is given by

$T_1 = t_2 - t_1 = 2^nT$ where n is the number of bits of ripple counter.

During T_1, output of integratorv_o is – ve going ramp voltage.

After T_1 control logic connects S_1 to $-V_R$. Now $-V_R$ is integrated and v_o is a + ve going ramp voltage. When v_o becomes zero at $t = t_3$ (say after N clock pulses), control logic issues EOC command.

Derivation:

$T_1 = t_2 - t_1 = 2^nT$ ….. (1)

$t_3 - t_2 = NT$ ….. (2)

For an integrator

$$v_o = -\frac{1}{RC}\int v_i dt \quad \text{….. (3)}$$

At $t = t_2$, $v_o = V_1$ (as shown in figure)

Here $v_i = v_a$

∴ Eq. (3) becomes

$$V_1 = -\frac{1}{RC}\int_{t_1}^{t_2} v_a\, dt = -\frac{v_a}{RC}(t_2 - t_1)$$

$$= -\frac{v_a}{RC}2^n\ T \qquad \{\text{From eq. (1)}\}$$

……. (4)

V_1 is given in terms of V_R as

$$V_1 = -\frac{1}{RC}\int_{t_3}^{t_2} -V_R\, dt = \frac{V_R}{RC}(t_2 - t_3)$$

$$= \frac{V_R}{RC}(-NT) \quad \{\text{using Eq. (2)}\}$$

$= -\frac{V_R NT}{RC}$ ….. (5)

Eqs. (4) and (5) ⇒

$-\frac{v_a}{RC} 2^n T = -\frac{V_R}{RC} NT$

i.e., $\mathbf{v_a = V_R\left(\frac{N}{2^n}\right)}$

Since V_R and n are constant, v_a is directly proportional to N and is independent of R, C and T.

Advantages of dual slope ADC:

(i) It is available in monolithic form, which is compatible with microprocessors and LED displays.

(ii) It provides excellent noise rejection.

(iii) Suitable for accurate measurement of slowly varying signals (e.g.: outputs of thermocouples and weighing scales)

(iv) Used in many instrumentation and control systems.

Disadvantage:

It has long conversion time (around 20 mSec). i.e., it is slow.

Problem 4.4: A dual slope ADC uses a 16–bit counter and a 4 MHz clock rate. The maximum i/p voltage is + 10 V. The maximum integrator o/p voltage should be – 8 V, when the counter has cycled through 2^n counts. The capacitor used in the integrator is 0.1 µF. Find the value of resistor R. Refer to Fig.8 (a).

Solution:

Clock period = $\frac{1}{4 \text{ MHz}} = \frac{1}{4 \times 10^6}$ Hz

$t_2 - t_1 = 2^n T = \frac{2^{16}}{4 \times 10^6} = 16.38$ mS

Output of integrator $v_o = -\frac{v_a}{RC} (t_2 - t_1)$

Given $v_o = -8$ V, $v_a = 10$ V and $C = 0.1 \times 10^{-6}$

$\therefore R = \frac{-1}{v_o C} v_a (t_2 - t_1)$

$= \frac{-1}{-8 \times 0.1 \times 10^{-6}} \times 10 \times 16.38 \times 10^{-3}$

= 205 Ω

Problem 4.5: If analog voltage in the problem 4.4 sis 4.129 V, find the equivalent digital number.

Solution:

$v_a = V_R\left(\frac{N}{2^n}\right)$

$\therefore N = \frac{v_a}{v_R} 2^n$

$= \left(\frac{4.129\ V}{8\ V}\right) 2^{16}$

= 33825

Above decimal value is equivalent to the binary value 1000010000100001

DAC/ADC SPECIFICATIONS

1. Resolution:

It is the smallest change in DAC output, when its i/p is changed. It is given as

Resolution = $\frac{V_{FS}}{2^N - 1}$ volts (= 1 LSB increment)

Where V_{FS} = Full scale o/p voltage

and n = number of bits

Resolution of ADC is defined as the smallest change in analog input for one-bit change at the o/p.

Example: For an 8–bit DAC with V_{FS} = 10 V,

Resolution = $\frac{10}{2^8 - 1}$ = 0.3922

% Resolution = Resolution x 100% = 39.22%

2. Linearity:

It tells how close is the actual o/p of a DAC to its ideal o/p. It is expressed as a fraction of LSB or % age of V_{FS}. It is determined by the fitted line passing through measured outputs.

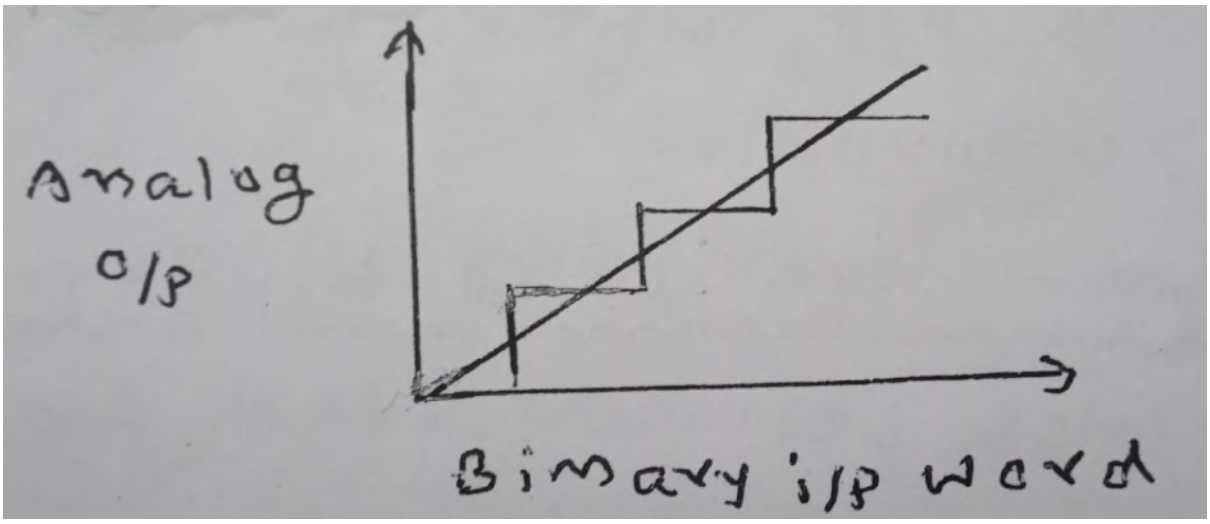


Fig. 9: Linearity

If the staircase o/p waveform is symmetrical w.r.t. the line as shown in Fig. 9, DAC is said to be linear. Otherwise, DAC is said to have linearity error.

3. Offset and Gain Errors:

Offset error is the o/p of DAC for a digital code, for which the o/p should be zero. Gain error is the difference in slope between the gain of ideal DAC and actual gain. They are indicated in Fig. 10 and Fig. 11 respectively.

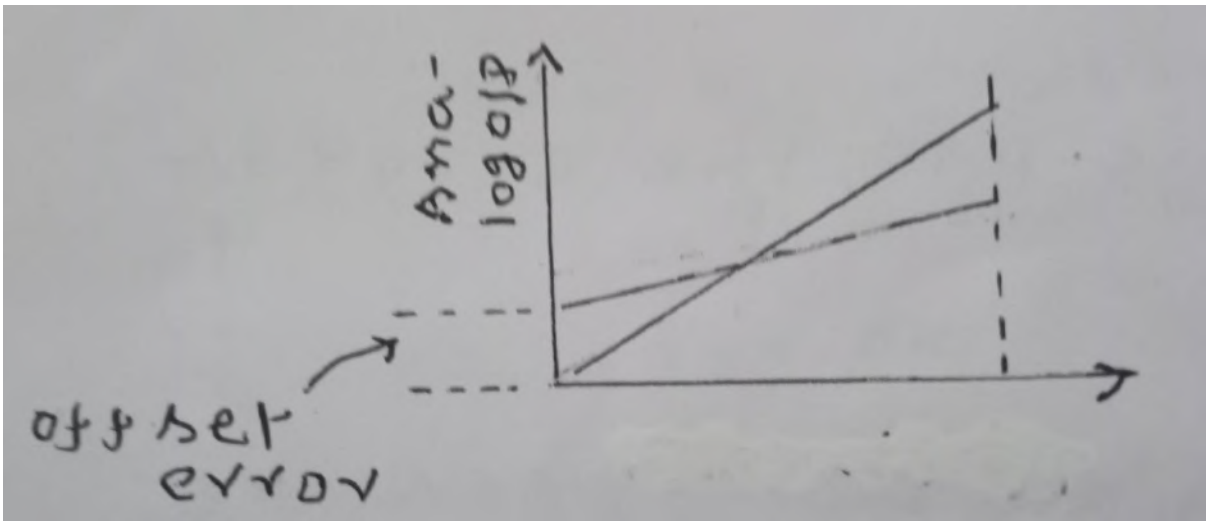


Fig. 10: Offset error

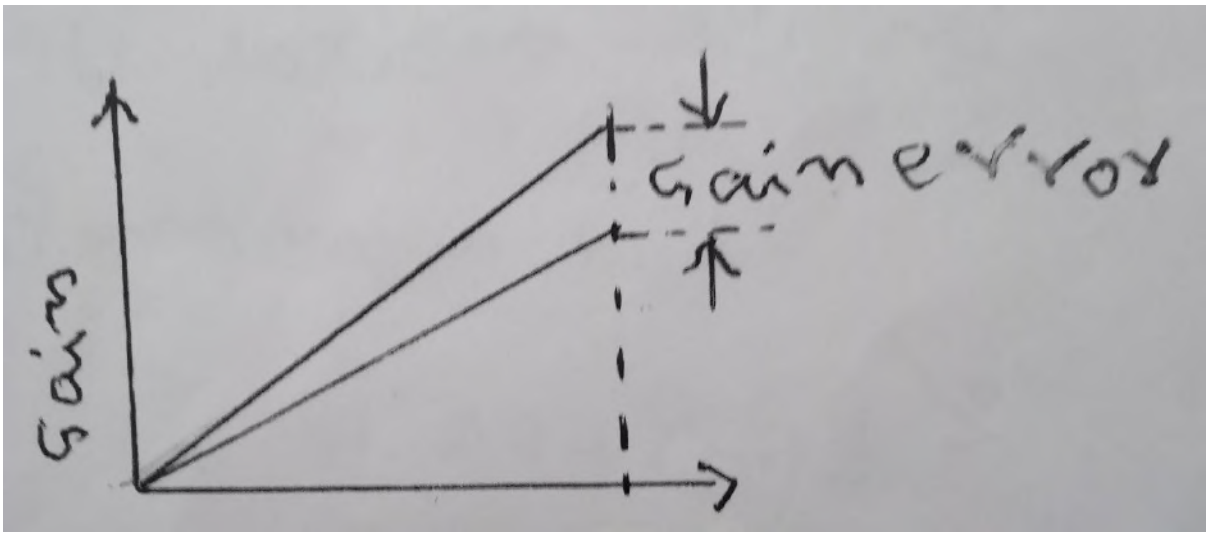


Fig. 11: Gain error

4. Settling Time:

It is the time taken by the DAC output to settle within a range of $\pm\left(\frac{1}{2}\right)$ LSB of its final value. It ranges from 100 nS to 10 μS.

5. Accuracy:

(i) Absolute Accuracy:

It is the maximum deviation between actual o/p and ideal o/p of a DAC.

(ii) Relative accuracy:

It is the maximum deviation between actual o/p and ideal o/p, when gain and offset errors are removed.

(iii) It is the difference between the ideal and measured o/p for successive binary i/p codes.

6. Monotonicity:

A monotonic DAC is a DAC whose analog o/p increases for increase in its digital i/p. For a monotonic DAC, the error is $<\pm\left(\frac{1}{2}\right)$ LSB.

All commercially available DACs are monotonic.

7. Stability:

The performance of a DAC changes with temperature, age and power supply variations. So, all its parameters must be specified over full temperature range.

****

VOLTAGE REGULATORS

A Voltage Regulator is a circuit that provides a constant voltage which is independent of variations in line voltage, load current and temperature.

SERIES OP–AMP REGULATOR

Classification of Voltage regulators:

Voltage regulators can be mainly classified as series (linear) and switching regulators.

In series regulator, a power transistor is connected between unregulated i/p and load. The transistor operates in active (linear region). So, it is also called linear regulator. Voltage drops across it is used to maintain constant voltage.

In switching regulator, a power transistor is used as a high frequency switch. i.e., power transistor operates in cutoff or saturation region. It doesn't conduct current continuously. This gives more efficiency than series regulators.

Comparison between series and switching regulators:

Series voltage regulators	Switching regulators
Few external parts required	More external parts
Simple design	Complicated design
Less noise	More noise
Less efficient	More efficient
More heat generation	Less heat generation
Only step–down operation is possible.	Step–up, step–down and – ve volt operations are possible

First 3 points are advantages and remaining are disadvantages.

SERIES OP-AMP REGULATOR:

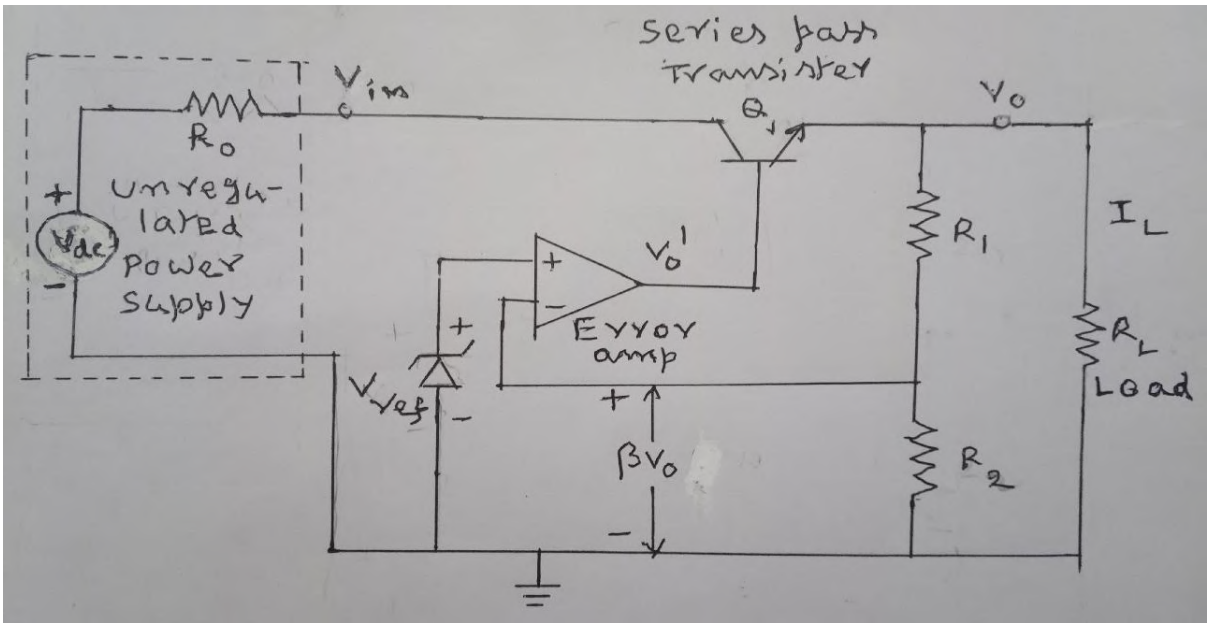


Fig. 1: Series OP–AMP regulator

A Voltage Regulator is a circuit that provides a constant voltage which is independent of variations inline voltage, load current and temperature.

Fig. 1 shows a regulated power supply using opamp. The circuit has 4 parts.

1. Reference Voltage Circuit (A Zener diode circuit)
2. Error Amplifier (An opamp)
3. Series Pass Transistor (A power transistor)
4. Feedback network (A voltage divider)

Let V_{in} = Unregulated input voltage input voltage

V_o =Regulated o/p voltage

Q_1 = power transistor acting as a series pass transistor

V_{ref} = Reference voltage

V_o' = Output of error amplifier (opamp)

R_1– R_2 = Voltage divider

Operation:

Q_1 is connected in series betweenV_{in} and V_o. Q_1 acts as an emitter follower. Thus, it provides sufficient current to drive the load. R_1– R_2 samples V_o. The sampled voltage is compared with V_{ref} obtained by Zener diode.

(V_{ref}–βV_o) is the input of error amplifier

v_o' is the o/p of error amplifier.

v_o' is used to drive Q_1.

If V_o increases, βV_o also increases, where $\beta = \frac{R_2}{R_1 + R_2}$. So, ($V_{ref} - \beta V_o$) reduces. Hence o/p of error amp also reduces.As a result, V_o reduces (Here $V_o = V_o'$ for emitter follower). Thus, the increase in v_o is nullified. Similarly, any decrease in V_o is also compensated.

IC VOLTAGE REGULATORS

Voltage regulators are available as monolithic ICs. They are mainly of 2 types: 3 terminal ICs and 723 General purpose IC

IC Voltage regulators can be available as:

(A) Three Terminal Fixed Voltage Regulators

1. Positive Voltage regulators (e.g.: 78XX series)
2. Positive Voltage regulators (e.g.: 79XX series)

(B) 723 General purpose Voltage Regulators

78XX (+ ve Voltage regulators):

They are fixed positive voltage regulators. XX is output voltage of the regulator. (XX = 5, 6, 8, 12, 15, 18 and 24 V). For example, 7808 has an o/p voltage of + 8 volts.

79XX (– ve Voltage regulators):

They are fixed negative voltage regulators. with output voltage options –5 V, –6 V, –8 V, –12 V, –15 V, –18 V, –24 V. For example, 7908 has an o/p voltage of – 8 volts.

Output options – 2 V and – 5.2 V are also available with 79XX series.

IC Voltage regulators are available in TO-3 (metal package) and TO-220 (Plastic package).

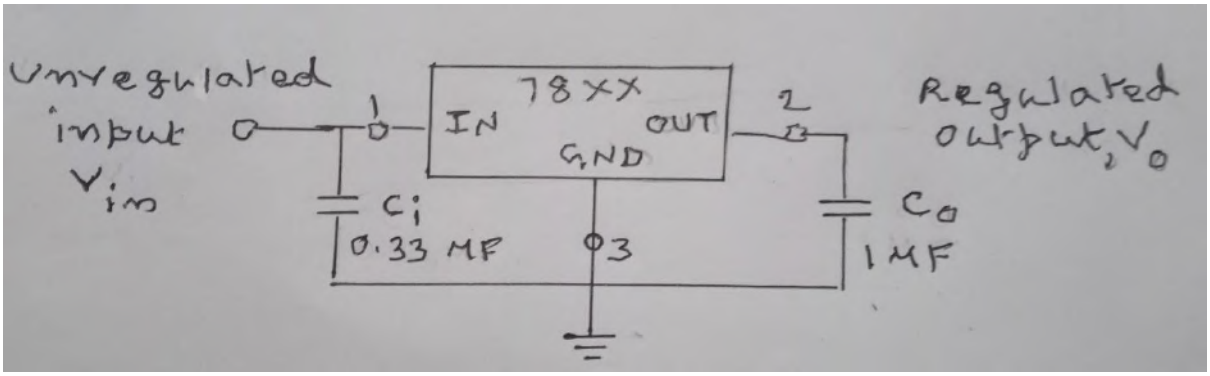


Fig. 2: A three terminal Voltage regulator

Fig. 2 shows a 3 terminal + ve IC Voltage regulator. Capacitor C_i is connected between input terminal and ground. Capacitor C_o is connected between output terminal and ground.

C_i is used to reduce the inductive effects due to long leads used. C_o is used improve transient response.

Important characteristics of 3 terminal IC regulators:

(i) They are available as 78XX series and 79XX series.

(ii) $V_{in} >= (V_o + 2)$ Volts (e.g.: If $V_o = 5$ V, then $V_{in} \geq 5+2$ (i.e., 7 V), where V_{in} = Unregulated input voltage input voltage and V_o = Regulated o/p voltage

(iii) Output current of voltage regulator can be varied from 0 up toits rated value $I_{o\,(max)}$. When it is $I_{o\,(max)}$, more heat is dissipated. So, heat sinks are provided to handle it.

(iv) IC has built in temperature sensor. It turns off IC when IC becomes too hot (when temperature > 125^0C). O/p current drops and remains thereuntil IC is cooled sufficiently.

Performance parameters of Voltage regulators:

1. Line regulation (or Input regulation)
2. Load Regulation
3. Ripple Rejection

1. Line regulation (or Input regulation):

It is the % change in V_o for a change in the i/p voltage V_{in}. It is expressed in mV or as % of V_o. Its typical value for 7805 is 3 mV.

2. Load Regulation:

It is the change in V_0 for a change in load current. It is expressed in mV or as a % of V_o. Its typical value for 7805 is 15 mV, for 5 mA < I_o< 1.5 A.

3. Ripple Rejection:

The voltage regulator can also reduce the amplitude of the ripple voltage. It is expressed in dB. Its typical value for 7805 is 78 dB.

723 GENERAL PURPOSE REGULATOR

Limitations of 3 terminal regulators:

1. No short circuit protection
2. Output (+ve or – ve) voltage is fixed

723 general purpose regulator can overcome the above limitations. It can be adjusted over a wide range of + ve or – ve regulated voltage. Boosting of current is also possible by connecting external components.

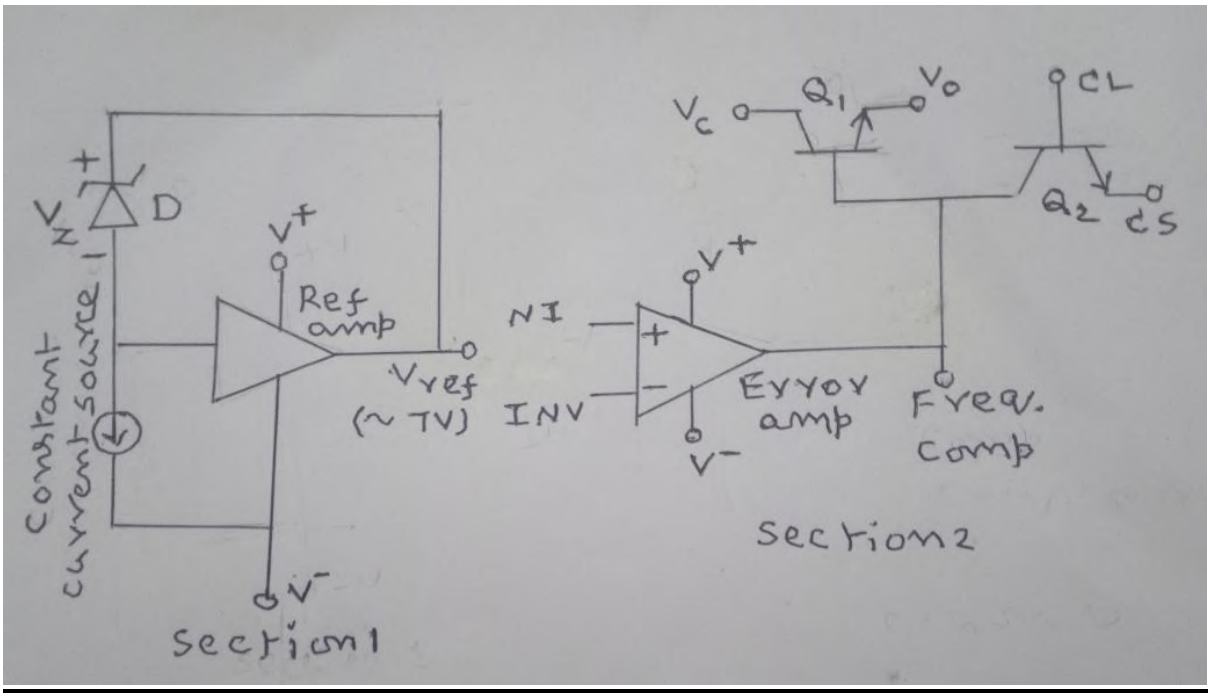


Fig. 3 (a): Functional Block Diagram of 723 regulator

Fig. 3 (a) shows the functional diagram of 723 regulator IC. It is available as 14-pin DIP package and 10-pin metal can package. It has 2 separate sections.

Section1: It contains Zener diode, constant current source and reference amplifier. It produces a fixed voltage of 7 V at the terminal V_{ref}. Because of constant current source, Zener diode outputs a fixed voltage.

Section2: It contains an error amplifier, a series pass transistor Q_1 and a current limit transistor Q_2. The error amplifier compares a sample of o/p voltage applied at the INV input terminal with a reference voltage V_{ref} applied at the NI input terminal. The error (difference) signal controls the conduction of Q_1.

These two sections are not connected internally. But IC provides the facility to connect.

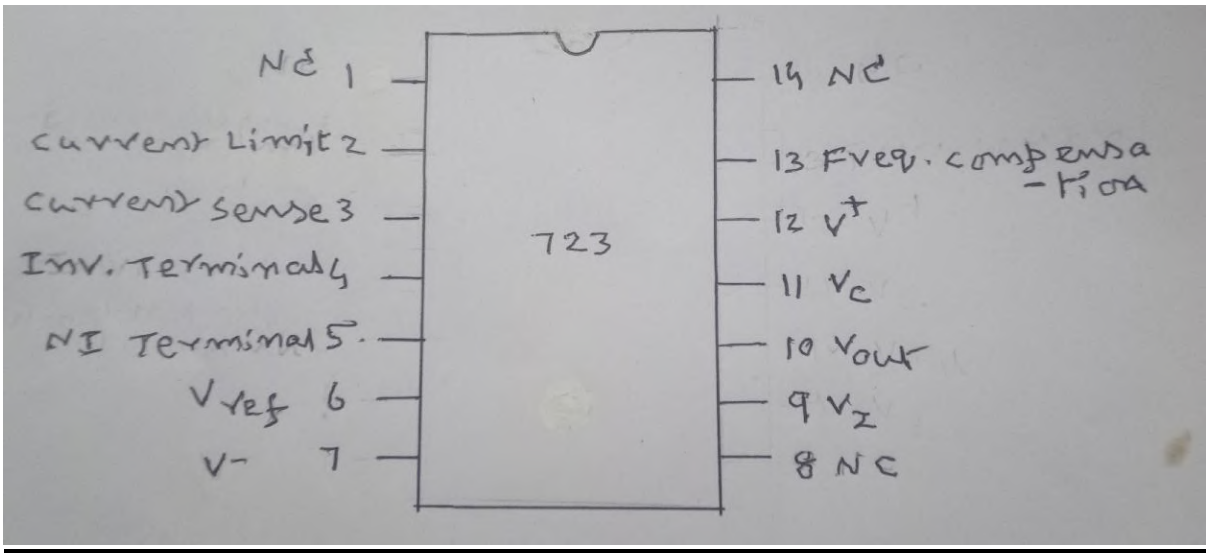


Fig. 3 (b): Pin Diagram of 14-pin DIP of 723

Fig. 3 (b) shows the pin diagram of 723 for a 14-pin DIP.

723 AS A LOW-VOLTAGE REGULATOR

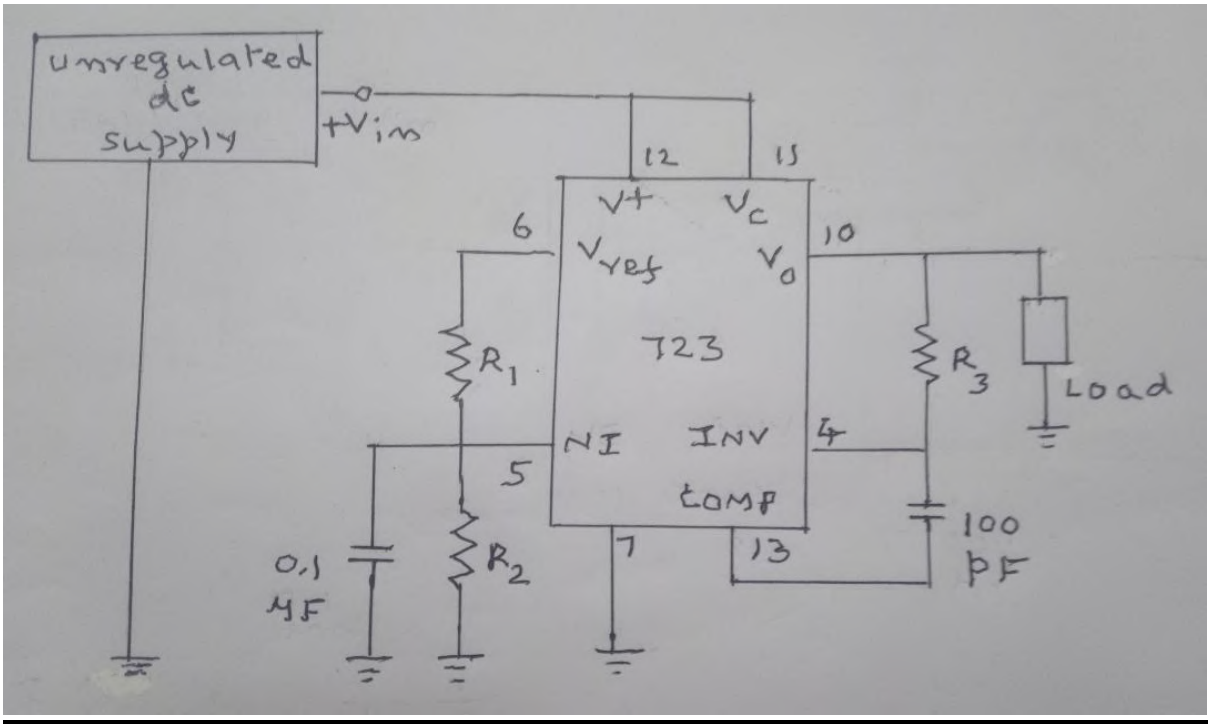


Fig. 4 (a): Pin Connections for a Low Voltage 723 Regulator

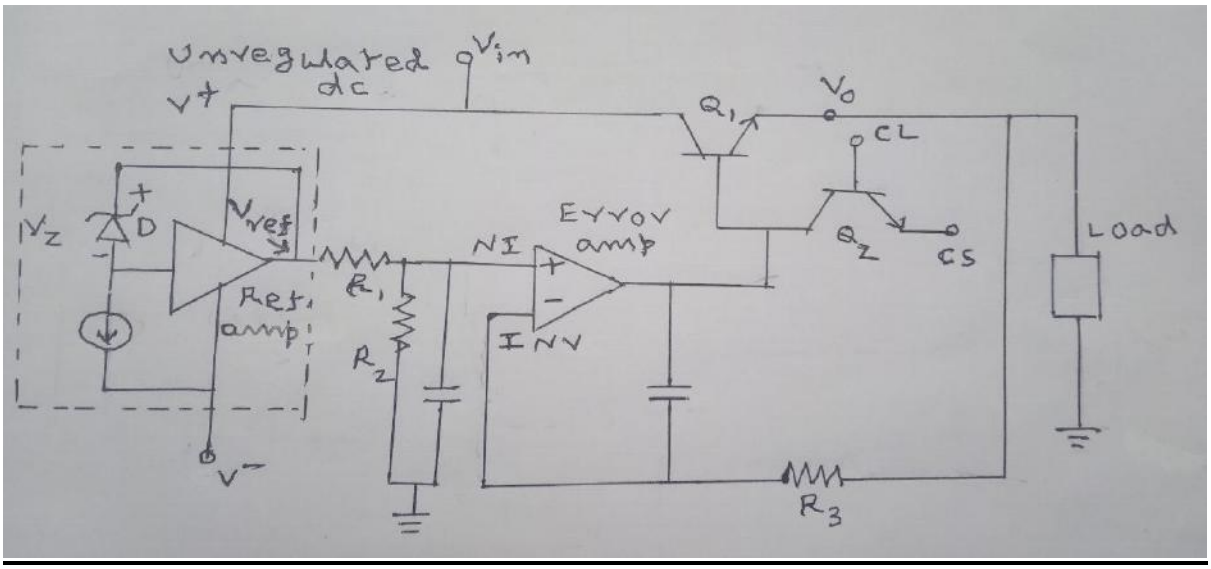


Fig. 4 (b): Functional Diagram for a Low Voltage Regulator

Fig. 4 (a) shows the schematic of 723 used as a low-voltage (2 to 7 V) regulator. V_{in} is the unregulated i/p and V_o is the regulated o/p. $V_o$is feedback to the INV terminal through R_3. V_{NI} is the voltage at the non-inverting terminal NI.

$V_{NI} = V_{ref}\frac{R_2}{R_1+R_2}$ (Here R_1-R_2 is acting as a voltage divider)

If V_o becomes low, voltage at INV also becomes low. So, input of error amplifier becomes high and so its o/p also becomes high. This output drives Q_1.So, voltage across load increases. Thus, initial drop in the load voltage is compensated. Similarly, any increase in the load voltage or changes in the input voltage are regulated.

Reference voltage is typically 7.15 V.

$\therefore V_o = 7.15 * \frac{R_2}{R_1+R_2} < 7.15$ V

Thus, the circuit acts as a low-voltage regulator (< 7 V)

The role of CL (Current limiting) and CS (Current sensing) terminals in Fig. 4 (b) is described below.

Current Limit Protection (Role of CL and CS)

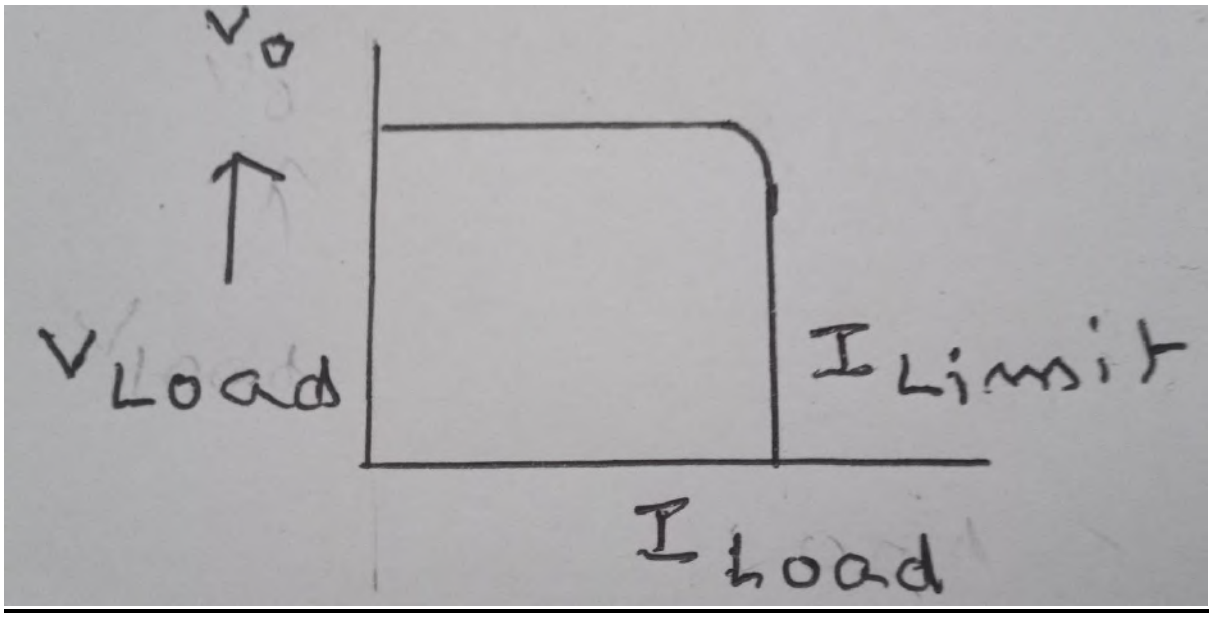


Fig. 5 (a) Characteristic Curve for Current Limiting

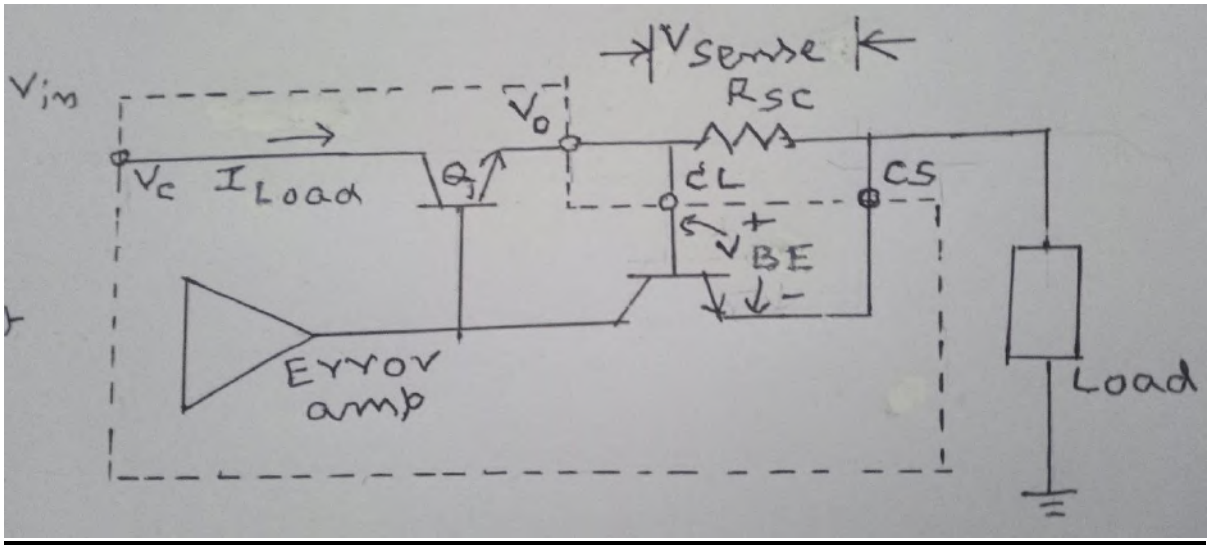


Fig. 5 (b) Current Limit Protection Circuit

The circuit in Fig. 4 (b) does not provide protection when current is large or under short circuit conditions. Circuit shown in Fig. 6 (b) provides such protection.

Current limiting refers to the ability of a regulator to prevent the load current from increasing above a preset value.

Fig. 5 (a) shows the characteristic curveof a current limited power supply. Here Output voltage remains constant up to I_{limit}. Beyond this point o/p voltage drops. The value of I_{limit} is set by connecting an external resistor R_{sc} between terminals CL and CS.

The CL terminal is also connected to output terminal V_o. CS terminal is connected to the load. It is not shown inf Fig. 5 (b).

The load current produces a small voltage drop V_{sense} drop across R_{sc}. This voltage is applied to base emitter junction of Q_2

When this voltage is nearly 0.6 V, transistor Q_2 tuns on

Now a part of the current from error amplifiergoes to the collector of Q_2. Thus, base current of Q_1 decreases. Hence emitter current of Q_1 reduces. Thus, any increase in load current will be nullified. Similarly, any decrease in load current is also compensated.

Here, $I_{limit} = \frac{V_{sense}}{R_{sc}} = \frac{0.5\ V}{R_{sc}}$

This method of current limiting is also called current sensing technique.

723 AS A HIGH-VOLTAGE REGULATOR

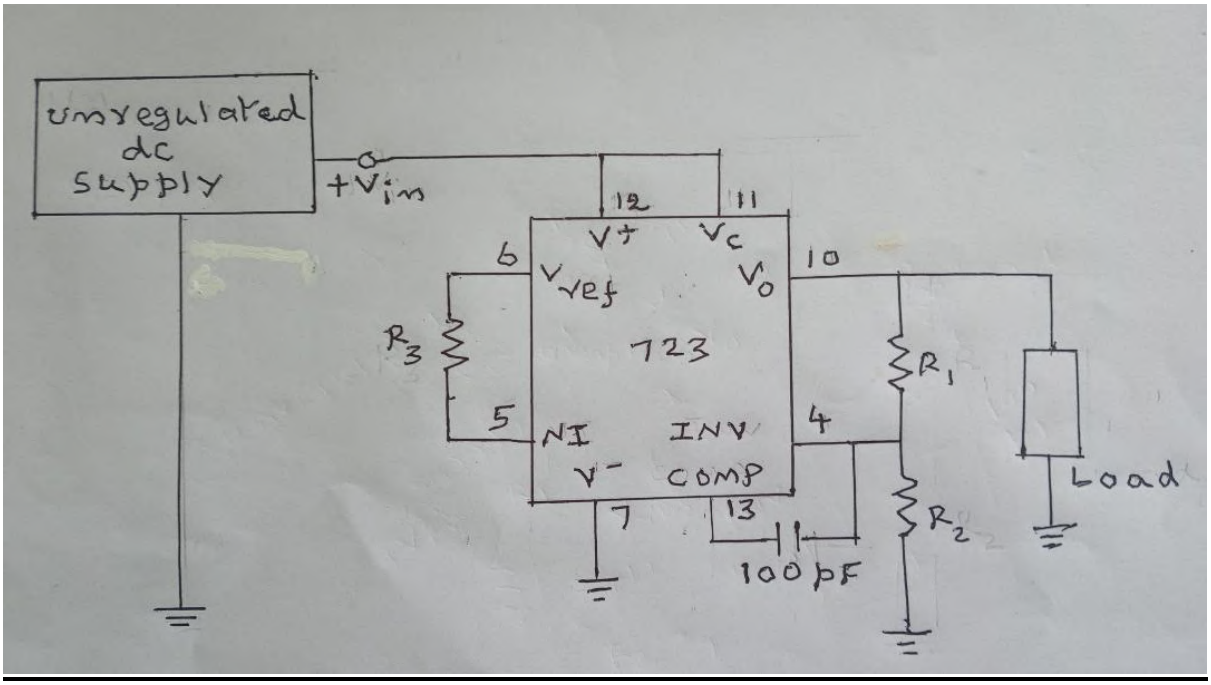


Fig. 6: High Voltage 723 Regulator

723 can also be used as a high voltage regulator to produce > 7 V.

Fig. 6shows the circuit of 723 used as high-voltage regular. Here the NI terminal is directly connected to V_{ref} through R_3. So, voltage at the NI terminal is V_{ref}.

The error amplifier operates in non-inverting mode. Its gain is given by

$A_v = 1 + \frac{R_1}{R_2}$

$\therefore V_o = 7.15\left(1 + \frac{R_1}{R_2}\right)$

SWITCHING REGULATORS (OR SWITCHED MODE REGULATORS)

In series regulator, a power transistor is connected between unregulated i/p and load. The transistor operates in active (linear region). So, it is also called linear regulator. Voltage drops across it is used to maintain constant voltage.

In switching regulator, a power transistor is used as a high frequency switch. i.e., power transistor operates in cutoff or saturation region. It doesn't conduct current continuously. Hence, the power transmitted across the pass transistor is in discrete pulses rather than as a steady current flow. When the device is cutoff, there is no current and so no power dissipation. In saturation region, thereis power dissipation, but it is less. This gives more efficiency than series regulators.

Switched voltage regulators rely on pulse width modulation (PWM) to control the average value of o/p voltage. The average value of a repetitive waveform depends on the area under the waveform. If the duty cycle is varied as shown in Fig. 7, the average value also changes correspondingly.

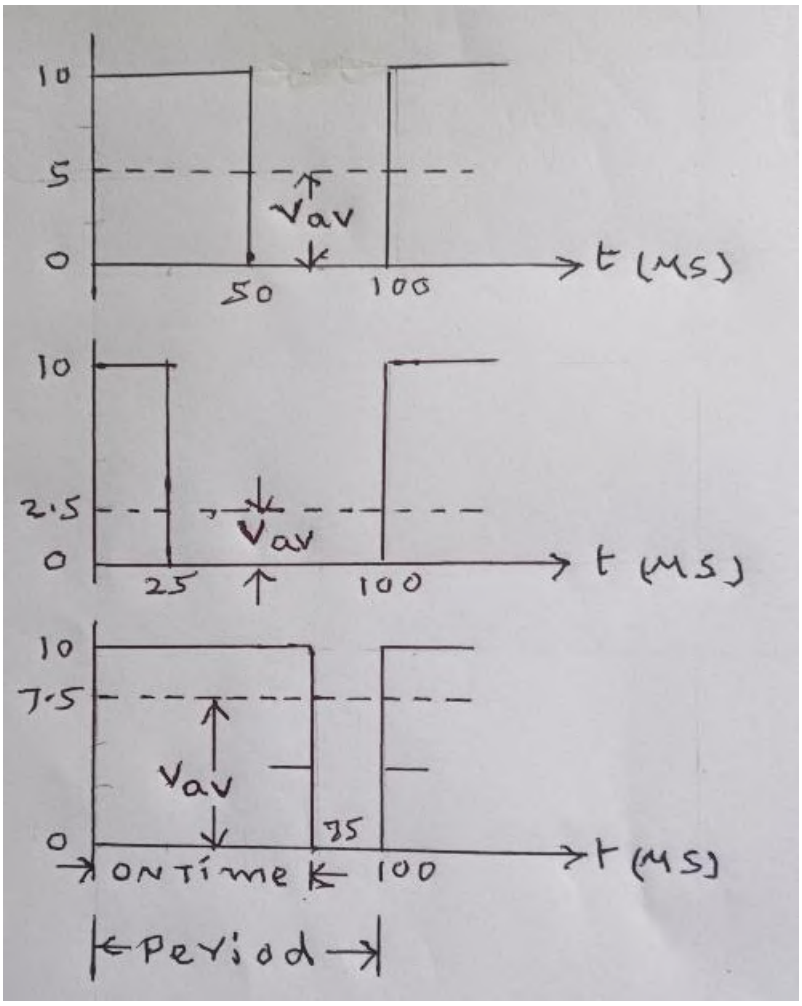


Fig. 7: PWM and Average Value

Advantages of Switching regulators over Series regulators:

1. More efficient
2. Less heat generation
3. Step–up, step–down and – ve volt operations are possible

Disadvantages of Switching regulators:

1. They need more external parts
2. Design is complex
3. More noisy

QUESTION BANK

Main Questions

1. Describe a binary weighted resistor type ADC. What are the drawbacks of it?
2. Describe a R–2R ladder type ADC. What are its drawbacks?
3. Describe a binary weighted resistor type ADC.

4. With the help of diagrams and truth tables, explain the operation of a flash type ADC.
5. With the help of necessary diagrams, explain the operation of a Successive approximation type ADC.
6. With the help of necessary diagrams, explain the operation of a Dual slope ADC. Mention its advantages and drawbacks.
7. Compare various DACs. Describe the specifications of DACs/ADCs.
8. Distinguish between series and switching regulators. Describe the functioning of series opamp regulator.
9. What is the need of 723 regulator? Describe the pin diagram and functional diagrams of the same.
10. Describe how IC 723 is used as low-voltage regulator.
11. Describe how IC 723 is used as high-voltage regulator.
12. Describe a switching regulator and pulse width modulation used by it.

2 Marks Questions

1. Describe the basic DAC/ADC technique.
2. What is the problem with binary weighted resistor type ADC?
3. What is the drawback of R–2R ladder ADC?
4. What are the advantages and disadvantages of a dual slope ADC?
5. Describe any two specifications of DACs/ADCs.
6. Mention the advantages of switching regulator. over series voltage regulators.
7. Mention the disadvantages of switching regulator. over series voltage regulators.
8. Define line regulation and load regulation.
9. What are the output voltage options available for 78XX/79XX?
10. What are the disadvantages of three terminal IC regulators?
11. Draw the pin diagram of 723.
12. Draw the pin diagram of a 78XX voltage regulator.

Objective Questions

51. What is the weightage of LSB in binary weighted/ R–2R ladder DAC?
    (a) $\frac{V_{FS}}{2}$ **(b)** $\boldsymbol{\frac{V_{FS}}{2^n}}$ (c) V_{FS} (d) None of the above
52. What is the weightage of MSB in binary weighted/ R–2R ladder DAC?
    (a) $\boldsymbol{\frac{V_{FS}}{2}}$ (b) $\frac{V_{FS}}{2^n}$ (c) V_{FS} (d) None of the above
53. Which type of DAC has less power dissipation?
    (a) Binary weighted DAC (b) R–2R ladder DAC **(c) Inverted R–2R ladder DAC** (d) Flash DAC
54. START and EOC commands are used in ——— type ADC.
    (a) Successive approximation ADC (b) Dual slope ADC **(c) Both**
    (d) They are used for only DACs

55.————— is the fastest type of ADC.

(a) Flash ADC (b) Counter type ADC(c) Dual slope DAC(d) Successive approximation ADC

56.Priority encoder is required in ————————— type of ADC.

(a) Parallel comparatorADC(b) Counter type ADC(c) Dual slope DAC(d) Successive approximation ADC

57.A 4–bit Successive approximation ADC needs —— clock pulses for A to D conversion process.

(a) 4**(b) 5**(c) 8(d) None

58.---------- is the difference in slope between the gain of ideal DAC and actual gain of DAC.

(a) Gain Error(b) Linearity error(c) Offset error (d) None

59.Which DAC acts in current mode?

(a) Binary weighted DAC(b) R–2R ladder DAC**(c) Inverted R–2R**

ladder DAC(d) Flash DAC

60.Output of DAC for a digital code, for which the o/p should be zero is called --------..

(a) Gain Error**(**b) Linearity error**(c) Offset error** (d) None

61.For 723 low voltage regulator, V_{ref}= ----------.

(a) 0 V**(b) 7.15 V**(c) 5 V(d) 10 V

62.In 723 DIP pack, output voltage is taken at pin ------.

(a) 3(b) 5 (c) 6 **(d) 10**

63.Unit for ripple rejection is ----------.

(a) mA**(**b) mV(c) No rejection**(d) dB**

64.Unit for Load rejection is ----------.

(a) mA**(b) mV**(c) No rejection(d) dB

65.Unit for Line rejection is ----------.

(a) mA**(b) mV**(c) No rejection(d) dB

66.In three-terminal + ve IC voltage regulator, pin 2 represents.

(a) Unregulated input**(b) Regulated output**(c) Ground (d) V_{CC}

67.Output of 7809 IC is ---------- Volts.

(a) 7 (b) 8**(c) 9**(d) - 9

68.Output of 7910 IC is ---------- Volts

(a) - **10**(b)10(c) - 7(d) - 9

69.Series pass transistor in series opamp regulator is used as ----------..

(a) Heat sink**(b) Emitter follower**(c) Load(d) None

70. If regulated output of a 3 terminal IC regulator is 4 V, the right choice for unregulated input is ----------.

(a) 3(b) 4(c) 5**(d) 6**

Topic from UNIT-2

SINUSOIDAL OSCILLATORS

Oscillator:

Oscillator is a circuit that produces an ac voltage or current waveform. The waveform may be sinusoidal or non-sinusoidal. In later case, it is normally called a waveform generator.

An oscillator doesn't need any input. It takes the energy from dc supply and converts it to ac signal. A sinusoidal oscillator can be realized by placing a frequency-selective network in the feedback path of an amplifier. The active device used in amplifier may be a transistor or opamp. Feedback is + ve feedback.

Types of Oscillators:

1. RC Phase Shift Oscillator
2. Wien Bridge Oscillator
3. Colpitt's Oscillator
4. Hartley Oscillator
5. Clap Oscillator
6. Crystal Oscillator

Principle of Oscillations (Barkhausen criterion):

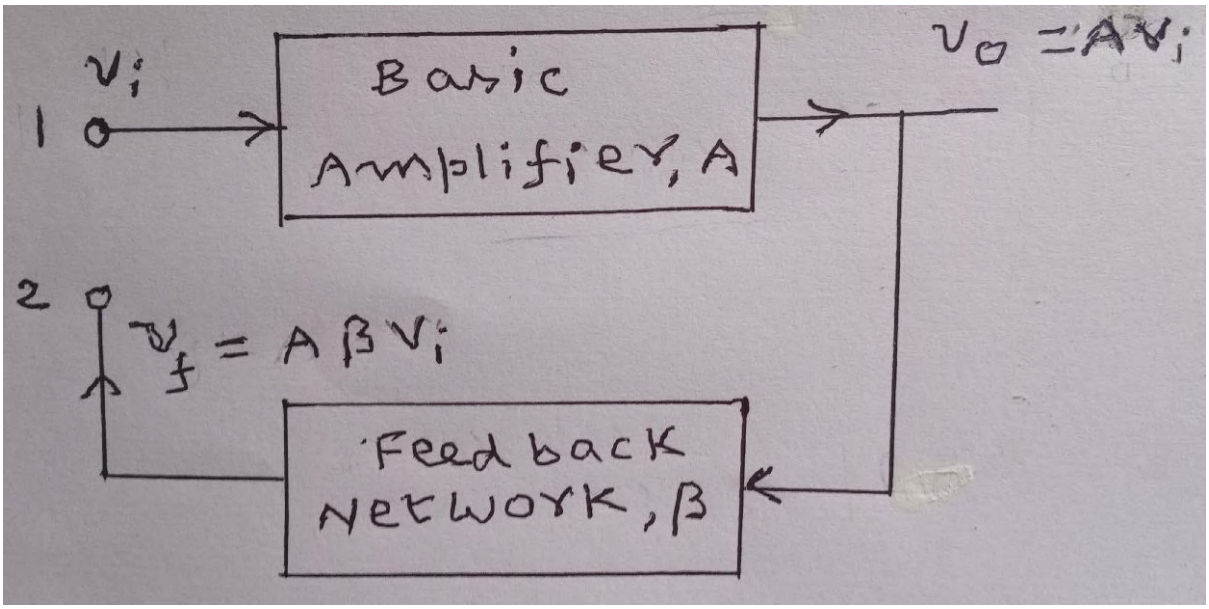


Fig. 1

Fig. 1 represents the basic schematic of an oscillator. Her

v_i = Input voltage

v_o = Output voltage

v_f = Feedback signal

A = Gain of basic amplifier

β = Gain of frequency selective network = feedback factor

Let the points 1 and 2 are not connected. Then let us apply the input signal v_i.

From Fig. 1, We get v_f = A β v_i

If the values of A and β are adjusted such that A β = 1 ,

Then $v_f = v_i$

Now let us connect points '1' and '2' and remove external signal v_i, the circuit will continue to provide same output, without external input.

Barkhausen Criteria:

There are two conditions to get oscillations. They are

|Aβ| = 1

<Aβ = 0^0 or multiple of 360^0

Above two conditions are called Barkhausen criteria.

First condition says that magnitude of loop gain Aβ is 1.

Second condition says that total phase shift of the circuit is 0^0 or multiple of

360^0.

Practical considerations:

Suppose Aβ is exactly 1. Then due to ageing, replacement of transistors, temperature, changes in circuit parameters Aβ may become < 1. Then gain (or o/p) of the circuit goes on decreasing. So, oscillations will die out. (1 to 5 %) So, Aβ is taken slightly more than unity. Then o/p will go on increasing. But it is limited by the non-linearity of active device. Thus o/p becomes constant when the active device enters saturation.

There is no ac input to an oscillator. It uses noise signal like switching transient as the initial input.

UNIT-5

Digital ICs

BASIC CMOS DIGITAL LOGIC GATE

One of the main disadvantages of the TTL logic series is that the gates are based on bipolar transistor logic technology and as transistors are current operated devices, they consume large amounts of power from a fixed +5 volt power supply. Also, TTL bipolar transistor gates have a limited operating speed when switching from an "OFF" state to an "ON" state and vice-versa called the "gate" or "propagation delay". To overcome these limitations complementary MOS called "CMOS" logic gates using "Field Effect Transistors" or FET's were developed.

As these gates use both P-channel and N-channel MOSFET's as their input device, at quiescent conditions with no switching, the power consumption of CMOS gates is almost zero, (1 to 2uA) making them ideal for use in low-power battery circuits and with switching speeds upwards of 100MHz for use in high frequency timing and computer circuits.

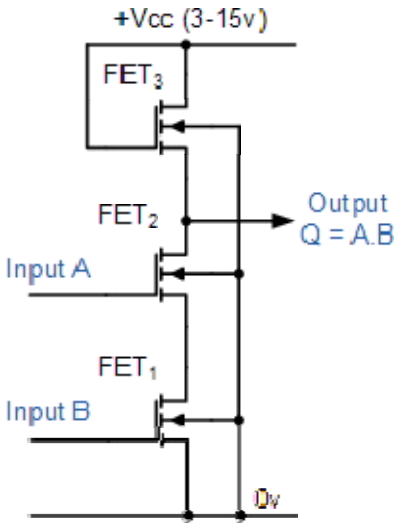


Fig6.5: 2-input NAND gate

This CMOS gate (fig 6.5) example contains 3 N-channel MOSFET's, one for each input FET_1 and FET_2 and one for the output FET_3. When both the inputs A and B are at logic level "0", FET_1 and FET_2 are both switched "OFF" giving output logic "1" from the source of FET_3. When one or both of the inputs are at logic level "1" current flows through the corresponding FET giving an output state at Q equivalent to logic "0", thus producing a NAND gate function.

For example, CMOS NAND gate:

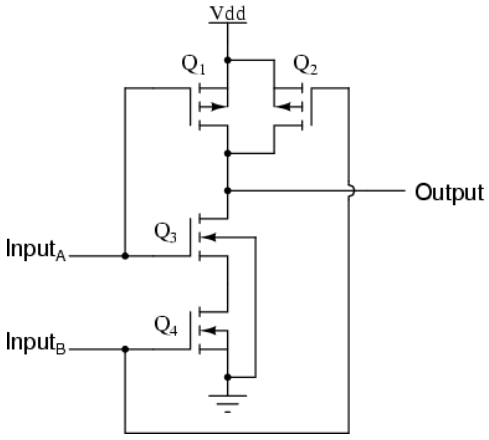


Fig 6.6: CMOS NAND gate

In fig 6.6 the transistors Q_1 and $Q_3$are series-connected complementary pair from the inverter circuit. Both are controlled by the same input signal (input A), the upper transistor turning off and the lower transistor turning on when the input is "high" (1), and vice versa. The transistors Q_2 and Q_4 are similarly controlled by the same input signal (input B), and how they will also exhibit the same on/off behaviour for the same input logic levels. The upper transistors of both pairs (Q_1 and Q_2) have their source and drain terminals paralleled, while the lower transistors (Q_3 and Q_4) are series-connected. What this means is that the output will go "high" (1) if *either* top transistor saturates, and will go "low" (0) only if *both* lower transistors saturate. The following sequence of illustrations shows the behaviour of this NAND gate for all four possibilities of input logic levels (00, 01, 10, and 11):

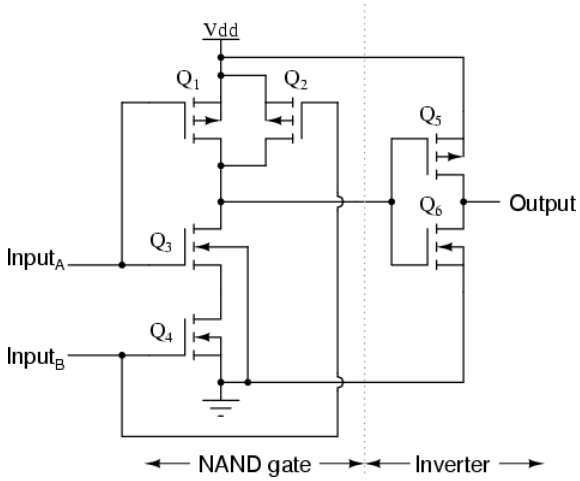


Fig 6.7 CMOS AND gate

A CMOS NOR gate circuit (fig 6.8) uses four MOSFETs just like the NAND gate, except that its transistors are differently arranged. Instead of two paralleled *sourcing* (upper) transistors

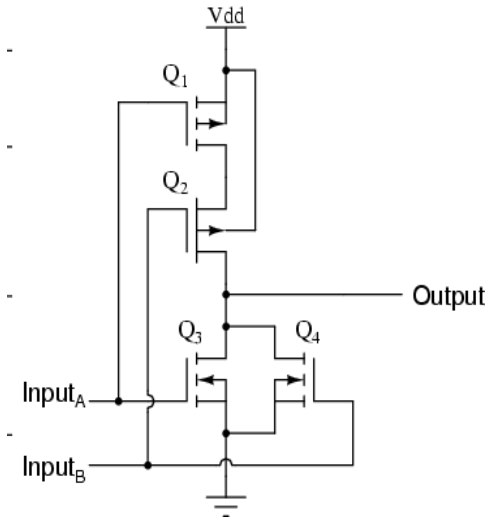


Fig 6.8: CMOS NOR Gate

connected to V_{dd} and two series-connected *sinking* (lower) transistors connected to ground, the NOR gate uses two series-connected sourcing transistors and two parallel-connected sinking transistors like this: As with the NAND gate, transistors Q_1 and Q_3 work as a complementary pair, as do transistors Q_2 and Q_4. Each pair is controlled by a single input signal. If *either* input A *or* input B are "high" (1), at least one of the lower transistors (Q_3 or Q_4) will be saturated, thus making the output "low" (0). Only in the event of *both* inputs being "low" (0) will both lower transistors be in cutoff mode and both upper transistors be saturated, the conditions necessary for the output to go "high" (1). This behavior, of course, defines the NOR logic function.

The OR function may be built up from the basic NOR gate with the addition of an inverter stage on the output (fig 6.9):

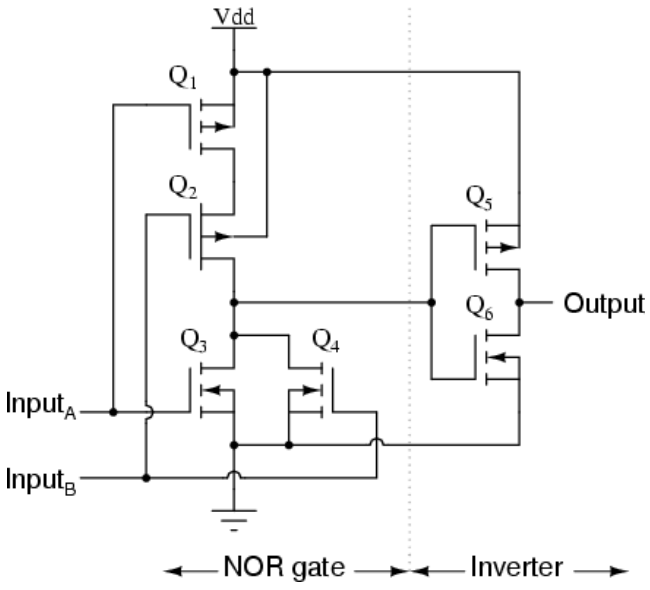


Fig 6.9: CMOS OR Gate

COMBINATIONAL CIRCUITS

Unlike Sequential Logic Circuitswhose outputs are dependent on both their present inputs and their previous output state giving them some form of Memory, the outputs of **Combinational Logic Circuits (fig 7.1)**are only determined by the logical function of their current input state, logic "0" or logic "1", at any given instant in time as they have no feedback, and any changes to the signals being applied to their inputs will immediately have an effect at the output. In other words, in a **Combinational Logic Circuit**, the output is dependant at all times on the combination of its inputs and if one of its inputs condition changes state so does the output as combinational circuits have "no memory", "timing" or "feedback loops".

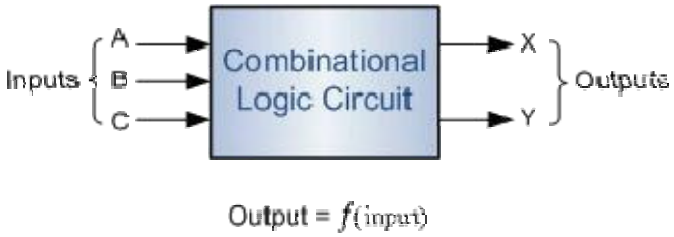


Fig 7.1 Block diagram of combinational circuits

Combinational Logic Circuits are made up from basic logic *NAND*, *NOR* or *NOT* gates that are "combined" or connected together to produce more complicated switching circuits. These logic gates are the building blocks of combinational logic circuits. An example of a combinational circuit is a decoder, which converts the binary code data present at its input into a number of different output lines, one at a time producing an equivalent decimal code at its output.

Combinational logic circuits can be very simple or very complicated and any combinational circuit can be implemented with only NAND and NOR gates as these are classed as "universal" gates. The three main ways of specifying the function of a combinational logic circuit are:

- Truth Table Truth tables provide a concise list that shows the output values in tabular form for each possible combination of input variables.
- Boolean Algebra Forms an output expression for each input variable that represents a logic "1"
- Logic Diagram Shows the wiring and connections of each individual logic gate that implements the circuit.

and all three are shown in fig 7.2.

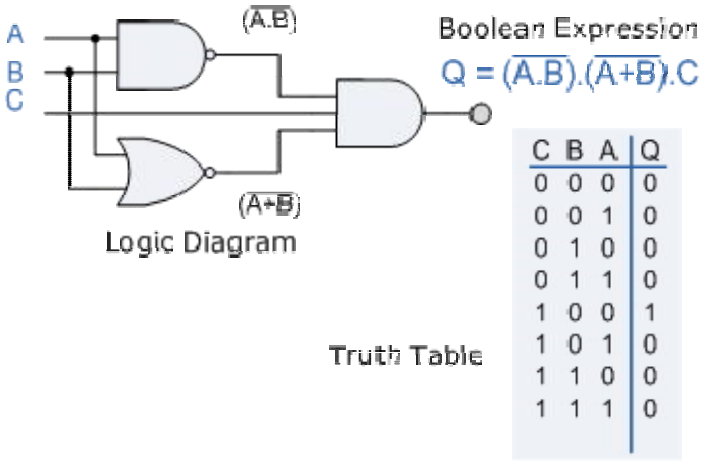


Fig 7.2 example of combinational circuit

As combinational logic circuits are made up from individual logic gates only, they can also be considered as "decision making circuits" and combinational logic is about combining logic gates together to process two or more signals in order to produce at least one output signal according to the logical function of each logic gate. Common combinational circuits made up from individual logic gates that carry out a desired application include Multiplexers, De-multiplexers, Encoders, Decoders, Full and Half Addersetc.

TTL-74XX & CMOS 40XX series ICs:

BIPOLAR 74XX

7400 series parts were constructed using bipolar transistors, forming what is referred to as transistor–transistor logic or **TTL**. Bipolar devices are also limited to a fixed power supply voltage, typically 5 V.As integrated circuits in the 7400 series were made in different technologies, usually compatibility was retained with the original TTL logic levels and power supply voltages.

- 74 - the "standard TTL" logic family had no letters between the "74" and the specific part number.
- 74L - Low power (compared to the original TTL logic family), very slow
- H - High speed (still produced but generally superseded by the S-series, used in 1970s era computers)
- S - Schottky (obsolete)
- LS - Low Power Schottky
- AS - Advanced Schottky
- ALS - Advanced Low Power Schottky
- F - Fast (faster than normal Schottky, similar to AS)

CMOS 40XX

The **40XX series** is a family of industry standard integrated circuits which implement a variety of logic functions using Complementary Metal–Oxide–Semiconductor technology, as a lower power and more versatile alternative to the 7400 series of TTL logic chips. Almost all IC manufacturers active during the era fabricated chips from this series.

4000 series parts had the advantage of lower power consumption, wider range of supply voltages (3 V to 15 V), and simpler circuit design due to the vastly increased fanout. However their slower speed (initially about 1 MHz operation, compared with bipolar TTL's 10 MHz) limited their applications to static or slow speed designs. Later, new fabrication technology largely overcame the speed problems, while retaining backward compatibility with most circuit designs. Although all semiconductors can be damaged by electrostatic discharge, the high impedance of CMOS inputs makes them more susceptible than bipolar transistor-based, TTL,

devices. Eventually, the advantages of CMOS (especially the later series such as 74HC) edged out the older TTL chips, but at the same time ever increasing LSI techniques edged out the modular chip approach to design.

- **Supply:** 3 to 15V, small fluctuations are tolerated.
- **Inputs** have very high impedance (resistance), this is good because it means they will not affect the part of the circuit where they are connected. However, it also means that unconnected inputs can easily pick up electrical noise and rapidly change between high and low states in an unpredictable way. This is likely to make the IC behave erratically and it will significantly increase the supply current. To prevent problems all unused inputs MUST be connected to the supply (either +Vs or 0V), this applies even if that part of the IC is not being used in the circuit!
- **Outputs** can sink and source only about 1mA if you wish to maintain the correct output voltage to drive CMOS inputs. If there is no need to drive any inputs the maximum current is about 5mA with a 6V supply, or 10mA with a 9V supply (just enough to light an LED). To switch larger currents you can connect a transistor.
- **Fan-out:** one output can drive up to 50 inputs.
- **Gate propagation time**: typically 30ns for a signal to travel through a gate with a 9V supply, it takes a longer time at lower supply voltages.
- **Frequency**: up to 1MHz, above that the 74 series is a better choice.
- **Power consumption** (of the IC itself) is very low, a few µW. It is much greater at high frequencies, a few mW at 1MHz for example.

Example common 40XX series chips

- 4000 - Dual 3-Input NOR Gate and Inverter
- 4001 - Quad 2-Input NOR Gate
- 4002 - Dual 4-Input NOR Gate OR Gate
- 4008 - 4-Bit Full Adder
- 4010 - hex non-inverting buffer
- 4011 - Quad 2-Input NAND Gate
- 4017 - Decade Counter / Johnson Counter
- 4511 - BCD to 7-segment LED driver

TTL ICS CODE CONVERTERS

In this section we will examine some methods of using combinational logic circuits to convert from one code to another.

BCD to BINARY CONVERSION:

One method of BCD to binary conversion uses adder circuits. This basic conversion process is as follows:

1. The value of each bit in the binary number is represented by a binary number
2. All the binary representations of the weights of the bits that are 1s in the BDC are added

3. The result of this addition is the binary equivalent of the BCD number

A more concise statement of this operation is:

The binary numbers representing the weights of the BCD bits are summed to produce the total binary number.

Let's examine an 8-bit BCD code (one that represents a 2-digit decimal numer) to understand the relationship between BCD and binary. For instance, you already know that the decimal number 87 can be expressed in BCD as

1000 0111

8 7

The left-most 4-bit group represents 80, and the right-most 4-bit group represents 7. That is, the left-most group has a weight of 10, and the right-most group has a weight of 10, and the right most group has a weight of 1.Within each group, the binary weight of each bit is as follows:

	Ten's digit				Units digit			
Weight	80	40	20	10	8	4	2	1
Bit Destination	B_3	B_2	B_1	B_0	A_3	A_2	A_1	A_0

The binary equivalent of each BCD bit is a binary number representing the weight of that bit within the total BCD number. This representation is given in Table 7.1.

BCD BIT	**BCD Weight**	**Binary Representation**						
		64	**32**	**16**	**8**	**4**	**2**	**1**
A0	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**1**
A1	**2**	**0**	**0**	**0**	**0**	**0**	**1**	**0**
A2	**4**	**0**	**0**	**0**	**0**	**1**	**0**	**0**
A3	**8**	**0**	**0**	**0**	**1**	**0**	**0**	**0**
B0	**10**	**0**	**0**	**0**	**1**	**0**	**1**	**0**
B1	**20**	**0**	**0**	**1**	**0**	**1**	**0**	**0**
B2	**40**	**0**	**1**	**0**	**0**	**0**	**0**	**0**
B3	**80**	**1**	**0**	**1**	**0**	**0**	**0**	**0**

Table 7.1

If the binary representations for the weights of all the 1s in the BCD number are added, the result is the binary number that corresponds to the BCD number.

Decimal Decoder using IC 74141

There are a number of possibilities for the representation of a decimal number into its equivalent binary code for example 8-4-2-1 and 2-4-2-1 codes are two of the most popular ones for binary code display (BCD). While the conversion of 8-4-2-1 BCD to decimal one is of most importance by the point of view of application. This conversion can be carried out with the use of TTL logic integrated circuits or by diode matrix. Here we will be discussing these two methods i.e.

1. Dotmatrixand
2. TTL logic system(transistor transistor logic)

BCD to decimal equivalent conversion using diode matrix system

This system i.e. **diode matrix system**(fig 7.3) can be implemented for the purpose of conversion of one number system to the other one with the help of a series of interconnected diodes. There when it is concerned about **conversion of a BCD code to its decimal equivalent** them there exists to ports one that four inputs i.e. 1,2,4,8 and upon switching of them it results into output of a decimal indicator showing a number from 0 to 9. When it is required to give a desired output decimal indicator there must not be any connection of the indicator to ground through diode because in that diode will make it short circuited. Now in order to give an output indicating the decimal 7 it will required input as:

- Input 1 set to 1 i.e. switched on
- Input 2 set to 1
- Input 4 set to 1
- Input 8 set to 0 i.e. switched off

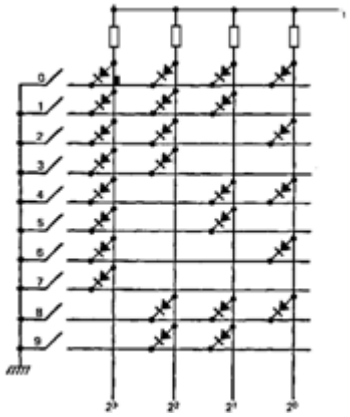


Fig 7.3 Dot Matrix System

As soon as the system receives these inputs it will result in indication of a decimal 7 at output. Because there all the output indicator circuits are so interconnected that upon application of this particular input it will short circuit all the other indicator circuits except that of 7 it will make the output to be set at 7 as will to retrieved too, at output. In this way there exist a particulars combination of inputs i.e. 1,2,4 and 8 for indication of each and every digit from 0 to 9.

Conversion of BCD code using TTL logic

There are a number of **bipolar integrator circuits** that were introduces in 1964 of the IC series 7400. And many decoder ICs are also there in market some of them are those of the series from 7441 to 7448 and also in TTL series it is 7400 series. There are some characteristics regarding the family that does not vary from one member to the other one that can be listed as:

- The output capabilities of the drive
- Characteristic regarding its switching
- The input loading if the device

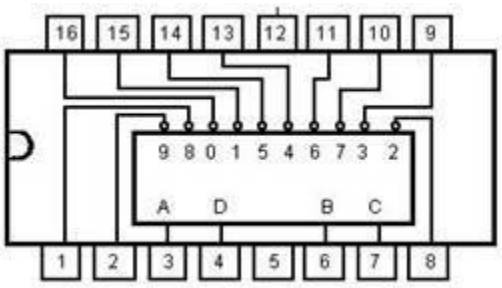


Fig 7.4 BCD to decimal conversion using TTL logic

Whereas the variations that make them differ from one to another is drive capability to suite the load applied to the output like whether it is going to be a nixie tube, seven segment displays or it is a LED display. The circuit (fig 7.4), which is generally implemented, uses **NAND gate circuit** in its circuitry which is adopted in most of the **TTL logic circuits**. Here 0 is the output which inverted in nature against the input logic 1. This 0 logic refers to a true condition while 1 stands for a false one which is in oppose of generality. The decoding of all the inputs is carried out explicitly. As the device is capable of decoding the decimal numbers from 0 to 1 so all the other decimal numbers i.e. from 10 to 15 obtains BCD code as false code of false logic. Here also, a particular binary code exists for each representation of each decimal number which is nothing but a combination of four bits. On application of 0010 it will result in production of decimal 2 similarly input 0011 will give its output as 3 in this way there are 16 combinations of these bits but only 10 of them are used for the **purpose of BCD conversion**. While the others ones i.e. from 1010 to 1111 all are used for the purpose of blanking the screen i.e. to make all the output terminals attain a zero value.

In spite of its feature of driving high power output the IC cannot be implemented for general

purpose indicating devices like a seven segment display.

Standard ICs for a combinational circuit

•Binary arithmetic circuits,

• Decoders,

• Encoders,

• Multiplexers,

• Code converters,

• Digital comparator for magnitude and equality,

• Parity generators and checkers2^n

• Bit wise ‘AND’, ‘OR’, ‘NOT’ logic processing

circuits.

DECODER

A Decoder is a multi-input, multi-output logic circuit (fig 7.5) which converts coded inputs into coded outputs, where the input and output codes are different. e.g. n-to-2^n, binary-coded decimaldecoders.

The encoded information is presented as a **n** inputs producing **2^n** possible outputs.

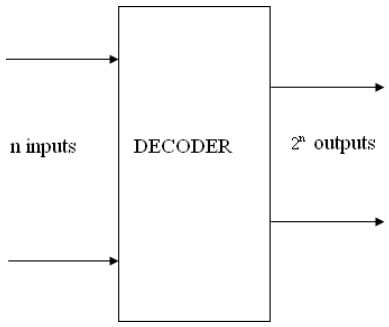
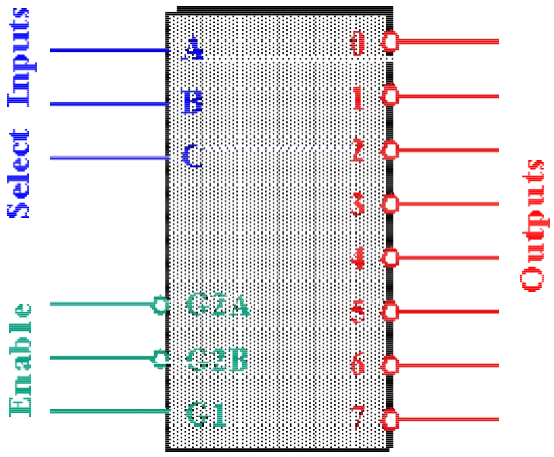


Fig 7.5 Block diagram of decoder

BINARY DECODER (74XX138 DECODER):

In the case of the 74xx138 (fig 7.6), these control lines consist of one active high control line (G1) and two active-low control lines (G2A, pin 4 and G2B). Thus, the 74xx138 will only

be in its 'decoding' mode if G1 is at logic '1' and G2A and G2B are at logic '0'. The 74xx138, whose generic product name is '3-to-8 Line Decoder/Multiplexer', obeys the truth table shown in Table 1. The outputs of the 74xx138 are 'active-low', i.e., the enabled output goes to logic '0' while all the other outputs are at logic '1'.

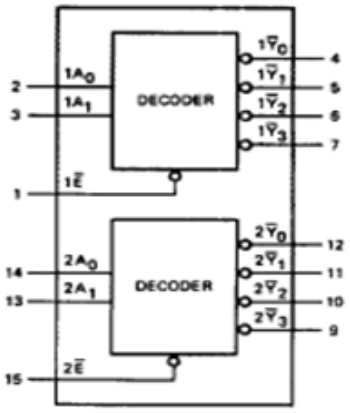


Inputs						Output							
Enable			Select										
G2A	G2B	G1	C	B	A	0	1	2	3	4	5	6	7
1	X	X	X	X	X	1	1	1	1	1	1	1	1
X	1	X	X	X	X	1	1	1	1	1	1	1	1
X	X	0	X	X	X	1	1	1	1	1	1	1	1
0	0	1	0	0	0	0	1	1	1	1	1	1	1
0	0	1	0	0	1	1	0	1	1	1	1	1	1
0	0	1	0	1	0	1	1	0	1	1	1	1	1
0	0	1	0	1	1	1	1	1	0	1	1	1	1
0	0	1	1	0	0	1	1	1	1	0	1	1	1
0	0	1	1	0	1	1	1	1	1	1	0	1	1
0	0	1	1	1	0	1	1	1	1	1	1	0	1
0	0	1	1	1	1	1	1	1	1	1	1	1	0

Fig 7.6: IC 74138 (3-8 decoder) logic symbol and functional truth table

THE 74XX139 DUAL 2-TO-4 DECODER:

The 74xx139 (fig 7.7) consist of two independent and identical 2-to-4 decoders. The enable inputs and outputs of IC 74xx139 are active LOW.



INPUTS			OUTPUTS			
$n\bar{E}$	nA_0	nA_1	$n\bar{Y}_0$	$n\bar{Y}_1$	$n\bar{Y}_2$	$n\bar{Y}_3$
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L

Fig.7.7 logic symbol and the functional table of IC 74xx139.

DEMULTIPLEXERS

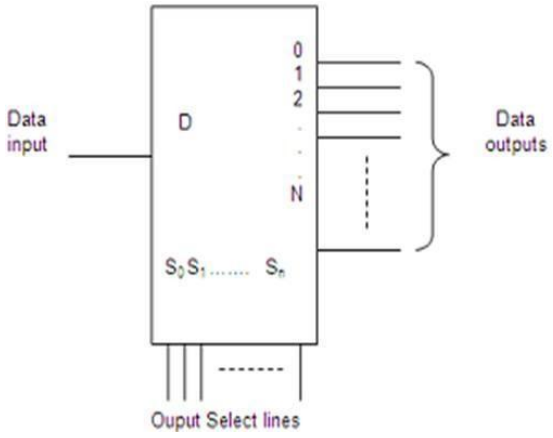


Fig 7.8 Logic symbol of demultiplexer

The logic symbol of a demultiplexer(as shown in fig 7.8) is a circuit that receives information on a single line and transmits this information on one of 2^n possible output lines. The selection of specific output line is controlled by the values of **n**selection lines. For example, each of the 16 outputs can be connected through a resistor and then through an LED to serve as a simple 16 LED controller. The LED can be chosen at random by the status of the 4 line selector inputs. However, due to the internal structure of the 74154, only one output can be enabled at a time. This chip is often used in demultiplexing applications, such as digital clocks, LED matrices, and other graphical outputs.

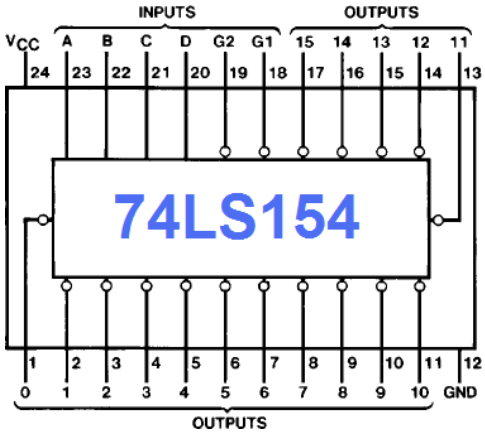


Fig 7.9a Pin Diagram of 74LS154

Function Table

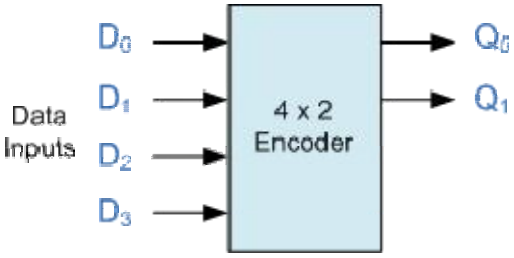
Inputs						Outputs														
G1	G2	D	C	B	A	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = High Level, L = Low Level, X = Don't Care

Table 7.2 Functional Truth Table of 74LS154

The pin diagram and functional truth table are shown in fig 7.9a and table 7.2. Each or these 4-line-to-16-line decoders utilize TTL circuitryto decode four binary-coded inputs into one of sixteenmutually exclusive outputs when both the strobe inputs, G1and G2, are low. The demultiplexing function is performedby using the 4 input lines to address the output line, passingdata from one of the strobe inputs with the other strobeinput low. When either strobe input is high, all outputs arehigh. These demultiplexers are ideally suited for implementinghigh-performance memory decoders. All inputs are bufferedand input clamping diodes are provided to minimizetransmission-line effects and thereby simplify system design.

ENCODER



Inputs				Outputs	
D_3	D_2	D_1	D_0	Q_1	Q_0
0	0	0	1	0	0
0	0	1	0	0	1
0	1	0	0	1	0
1	0	0	0	1	1
0	0	0	0	x	x

Fig 7.10: 4-to-2 Binary Encoder(2^nxn)

An encoder is a digital circuit that performs the inverse operation of a decoder. An encoder has 2^n input lines and n output lines. An example of 4-2 line encoder is shown in fig 7.10. In encoder the output lines generate the binary code corresponding to the input valueOne of the main disadvantages of standard digital encoders is that they can generate the wrong output code when there is more than one input present at logic level "1". For example, if we make inputs D_1 and D_2 HIGH at logic "1" at the same time, the resulting output is neither at "01" or at "10" but will be at "11" which is an output binary number that is different to the actual input present. Also, an output code of all logic "0"s can be generated when all of its inputs are at "0" OR when input D_0 is equal to one.

THE 74XX147 (DECIMAL TO BCD ENCODER):

The decimal to BCD encoder, usually has ten input lines and four output lines. Fig 7.11a and table 7.3 shows the logic symbol for IC 74xx147 and its functional truth table. It has 4 input lines and 4 output lines. Both input and output lines are asserted active LOW. If all input lines are 1 then all outputs are 1.

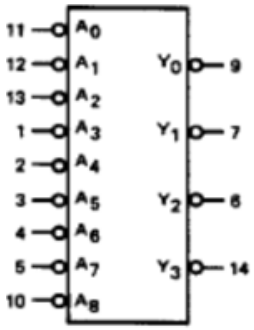


Fig 7.11a: Pin diagram of 74LS147

FUNCTION TABLE

INPUTS									OUTPUTS			
$\overline{A}_0$	$\overline{A}_1$	$\overline{A}_2$	$\overline{A}_3$	$\overline{A}_4$	$\overline{A}_5$	$\overline{A}_6$	$\overline{A}_7$	$\overline{A}_8$	$\overline{Y}_3$	$\overline{Y}_2$	$\overline{Y}_1$	$\overline{Y}_0$
H	H	H	H	H	H	H	H	H	H	H	H	H
X	X	X	X	X	X	X	X	L	L	H	H	L
X	X	X	X	X	X	X	L	H	L	H	H	H
X	X	X	X	X	X	L	H	H	H	L	L	L
X	X	X	X	X	L	H	H	H	H	L	L	H
X	X	X	X	L	H	H	H	H	H	L	H	L
X	X	X	L	H	H	H	H	H	H	L	H	H
X	X	L	H	H	H	H	H	H	H	H	L	L
X	L	H	H	H	H	H	H	H	H	H	L	H
L	H	H	H	H	H	H	H	H	H	H	H	L

Table 7.3Functional truth table of 74LS147

7.6.1 PRIORITY ENCODER:

The level of each input pin and if there was more than one input at logic level "1" the actual output code would only correspond to the input with the highest designated priority. Then this type of digital encoder is known commonly as a **Priority Encoder** or **P-encoder** for short.

If a multiplexer or encoder has N output lines, then it has 2^N input lines. A common example of a decoder/demultiplexer IC is the 74LS148, which is a Low-Power Schottky TTL device that has 8 input lines and 3 output lines. The 74LS148 is a priority encoder, which means that if more than one of its inputs are active, then the active input line with the highest binary weight will be given priority, and the output of the encoder will depend on this prioritized input. Table 7.4 shows the truth table for the 74LS148. Note that E0 and GS are output pins while E1 is a control pin (input).

Priority encoders are available in standard IC form and the TTL 74LS148 is an 8-to-3 bit priority encoder which has eight active LOW (logic "0") inputs and provides a 3-bit code of the highest ranked input at its output. Priority encoders output the highest order input first for example, if input lines "D2", "D3" and "D5" are applied simultaneously the output code would be for input "D5" ("101") as this has the highest order out of the 3 inputs. Once input "D5" had been removed the next highest output code would be for input "D3" ("011"), and so on.

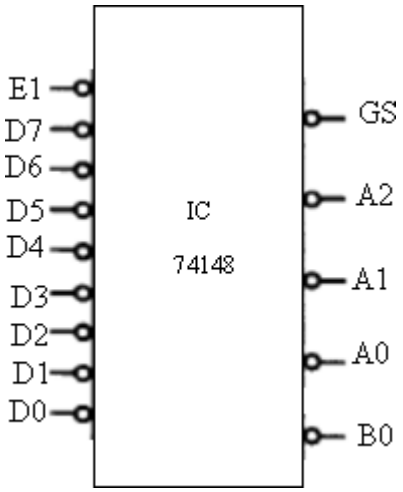


Fig 7.12 Pin Diagram of 74148

The IC 74xx148 (fig 12) is an 8-input priority encoder. It accepts data from eight active low inputs and provides a binary representation on the three active low outputs. A priority is assigned to each input so that when two or more inputs are simultaneously active, the input with the highest priority represented on the output. Input D0 has the least priority and input D7 has highest priority.

The truth table for IC 74138, 8-to-3 bit priority encoder is given as table 7.4:

E1	D7	D6	D5	D4	D3	D2	D1	D0	A2	A1	A0	E0	GS
1	X	X	X	X	X	X	X	X	1	1	1	1	1
0	1	1	1	1	1	1	1	1	1	1	1	0	1
0	0	X	X	X	X	X	X	X	0	0	0	1	0
0	1	0	X	X	X	X	X	X	0	0	1	1	0
0	1	1	0	X	X	X	X	X	0	1	0	1	0
0	1	1	1	0	X	X	X	X	0	1	1	1	0
0	1	1	1	1	0	X	X	X	1	0	0	1	0
0	1	1	1	1	1	0	X	X	1	0	1	1	0
0	1	1	1	1	1	1	0	X	1	1	0	1	0
0	1	1	1	1	1	1	1	0	1	1	1	1	0

Table 7.4 Truth Table of 74148

MULTIPLEXERS AND THEIR APPLICATIONS:

A **multiplexer** (or **mux**) is a device that selects one of several analog or digital input signals and forwards the selected input into a single line. A multiplexer of 2^n inputs has n select lines, which are used to select which input line to send to the output (fig 7.13). Multiplexers are mainly used to increase the amount of data that can be sent over the network within a certain amount of time and bandwidth. A multiplexer is also called a **data selector**. An electronic multiplexer can be considered as a multiple-input, single-output switch.

The following table 7.5 shows different multiplexer Ics

	IC No.	Function	Output State
1	74157	Quad 2:1 mux.	Output same as input given
2	74158	Quad 2:1 mux.	Output is inverted input
3	74153	Dual 4:1 mux.	Output same as input
4	74352	Dual 4:1 mux.	Output is inverted input
5	74151A	8:1 mux.	Both outputs available (i.e., complementary outputs)
6	74151	8:1 mux.	Output is inverted input
7	74150	16:1 mux.	Output is inverted input

Table 7.5 Multiplexer Ics

THE 74XX151 (8 TO 1 MULTIPLEXER)

The 74xx151 (fig 7.14) is a 8-to-1 multiplexer. It has eight inputs. It provides two outputs, one is the active HIGH, the other is active LOW. It contain 3 select inputs C, B and A which select one of the eight inputs. The 74xx151 is provided with active low enable input.

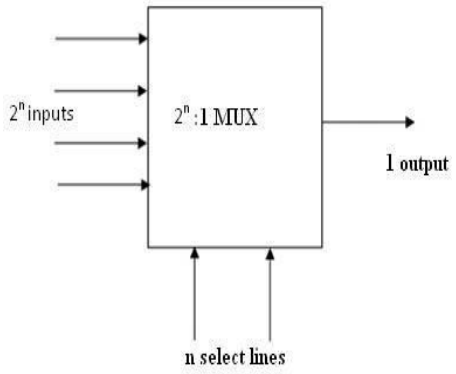


Fig 7.13 Logic symbol of multiplexer

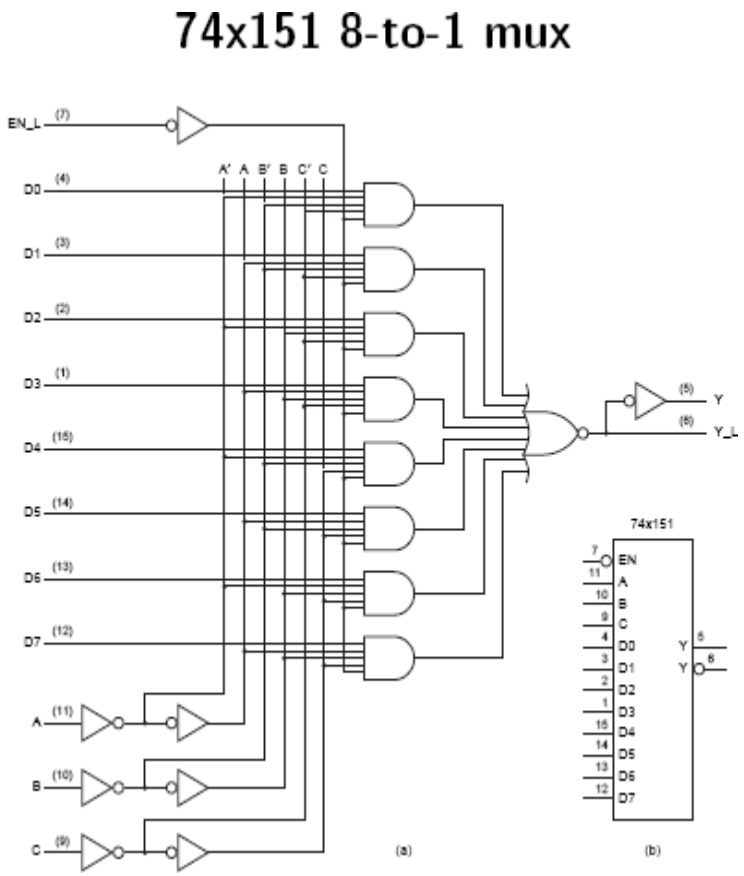


Fig 7.14: 74151 8-to-1 Mux

Inputs				Outputs	
EN_L	C	B	A	Y	Y_L
1	x	x	x	0	1
0	0	0	0	D0	D0′
0	0	0	1	D1	D1′
0	0	1	0	D2	D2′
0	0	1	1	D3	D3′
0	1	0	0	D4	D4′
0	1	0	1	D5	D5′
0	1	1	0	D6	D6′
0	1	1	1	D7	D7′

Table 7.6: Truth table for 74151 mux

THE 74XX157 QUAD 2-INPUT MULTIPLEXER:

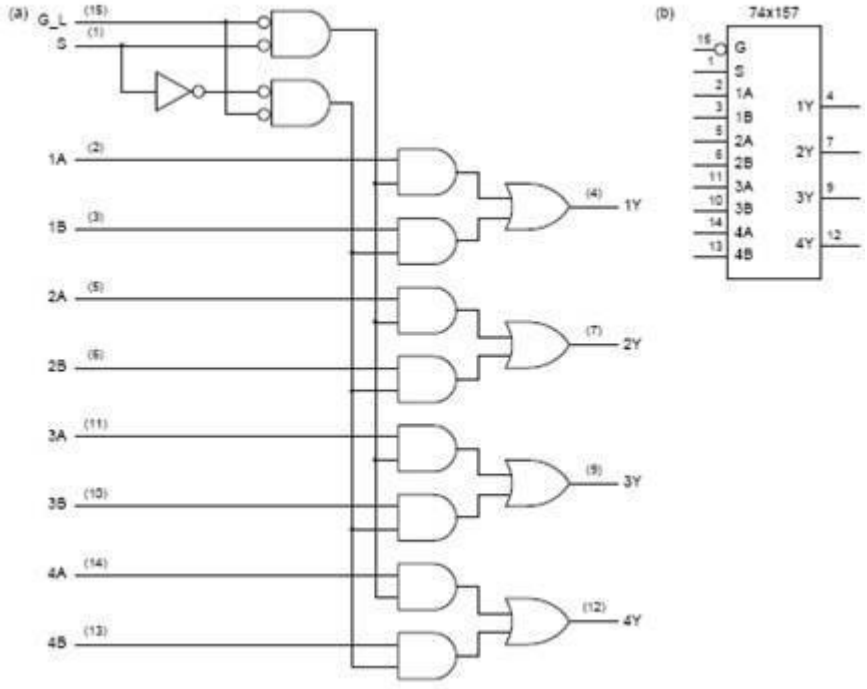


Fig 7.15 Logic symbol and logic circuit diagram of IC 74157

The IC 74xx157 shown in fig 7.15 is a quad 2-input multiplexer which selects four bits of data from two sources under the control of a common select input(S), the Enable input($E^{'}$) is active LOW. When $E^{'}$ is HIGH, all of the outputs (Y) are forced low regardless of all other input conditions. The truth table is shown in table 7.7

Inputs		Outputs			
G_L	S	1Y	2Y	3Y	4Y
1	x	0	0	0	0
0	0	1A	2A	3A	4A
0	1	1B	2B	3B	4B

Table 7.7: Truth table of 74157

PARALLEL BINARY ADDER (IC 74LS83/74LS283):

4-bit parallel adders that are available in IC form are the 74LS83A and the 74LS283 low power Schottky TIL devices. The 74LS83A and the 74LS283 are function- Schottky TIL devices. The 74LS83A and the 74LS283 are functionally identical to each other but not pin compatible; that is, the pin numbers for the inputs and outputs are different due to different power and ground pin connections. For the 74LS283, Vccand ground is pin 8, which is a more standard configuration. Pin diagrams symbols for both of these devices are shown, with symbols, in Fig7.16 and fig 7.17. The functional truth tables are shown in tables 7.8 and 7.9.

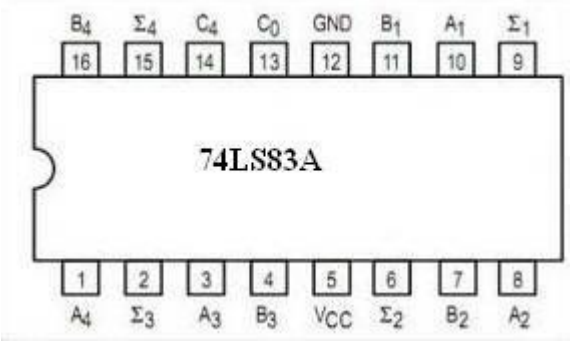


Fig 7.16Pin diagram of 74LS83A

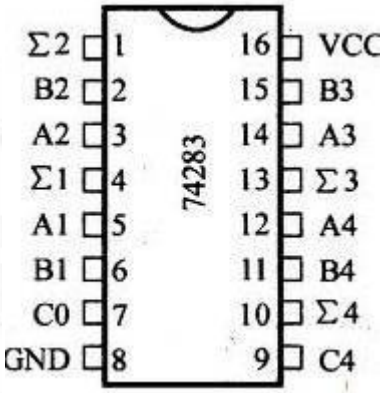


Fig 7.17 Pin diagram of 74283

Functional discription of 74LS83A

The LS83A adds two 4-bit binary words (A plus B) plus the incoming carry. The binary sum appears on the sum outputs (R1–R4) and outgoing carry (C4) outputs.

$$C0 + (A1+B1)+2(A2+B2)+4(A3+B3)+8(A4+B4) = R1+2R2+4R3+8R4+16C4$$

Where: (+) = plus

Due to the symmetry of the binary add function the LS83A can be used with either all inputs and outputs active HIGH (positive logic) or with all inputs and outputs active LOW (negative logic). Note that with active HIGH Inputs, Carry Input cannot be left open, but must be held LOW when no carry in is intended.

For example:

	C_0	A_1	A_2	A_3	A_4	B_1	B_2	B_3	B_4	Σ_1	Σ_2	Σ_3	Σ_4	C_4
Logic Levels	L	L	H	L	H	H	L	L	H	H	H	L	L	H
Active HIGH	0	0	1	0	1	1	0	0	1	1	1	0	0	1
Active LOW	1	1	0	1	0	0	1	1	0	0	0	1	1	0

FUNCTIONAL TRUTH TABLE

$C_{(n-1)}$	A_n	B_n	Σ_n	C_n
L	L	L	L	L
L	L	H	H	L
L	H	L	H	L
L	H	H	L	H
H	L	L	H	L
H	L	H	L	H
H	H	L	L	H
H	H	H	H	H

C_1 — C_3 are generated internally
C_0 — is an external input
C_4 — is an output generated internally

Table 7.8 Functional truth table of 74LS83

Input				Outputs					
				When C0 = L			When C0 = H		
				When C2 = L			When C2 = H		
A1 / A3	B1 / B3	A2 / A4	B2 / B4	Σ1 / Σ3	Σ2 / Σ4	C2 / C4	Σ1 / Σ3	Σ2 / Σ4	C2 / C4
L	L	L	L	L	L	L	H	L	L
H	L	L	L	H	L	L	L	H	L
L	H	L	L	H	L	L	L	H	L
H	H	L	L	L	H	L	H	H	L
L	L	H	L	L	H	L	H	H	L
H	L	H	L	H	H	L	L	L	H
L	H	H	L	H	H	L	L	L	H
H	H	H	L	L	L	H	H	L	H
L	L	L	H	L	H	L	H	H	L
H	L	L	H	H	H	L	L	L	H
L	H	L	H	H	H	L	L	L	H
H	H	L	H	L	L	H	H	L	H
L	L	H	H	L	L	H	H	L	H
H	L	H	H	H	L	H	L	H	H
L	H	H	H	H	L	H	L	H	H
H	H	H	H	L	H	H	H	H	H

Table 7.9 Functional truth table of 74283

PARALLEL BINARY SUBTRACTOR USING 2'S COMPLEMENT SYSTEM

The problem of subtraction gets converted into that of addition if l's and 2's complement representation are used for representing negative numbers. The algorithm for a subtractor using adder is given in Fig.7.18a.The two numbers A and *B* can be of the same sign or of opposite signs. If the two numbers are of unlike sign, we may come across the problem of *overflow* or *underflow*. Overflow occurs when the subtraction operation produces a number larger than the largest possible number which can be represented by n-bits. On the other hand, underflow occurs when the result produced is smaller than the smallest number which can be represented by *n-bits.*The overflow and underflow logic is illustrated in Fig.7.18. The subtractor circuit is given in Fig. 7.18b. The reader can verify the operation of this circuit. If overflow or underflow occurs then the result is wrong. This circuit can be converted into an ADDER/SUBTRACTOR circuit with ADD/SUB control.

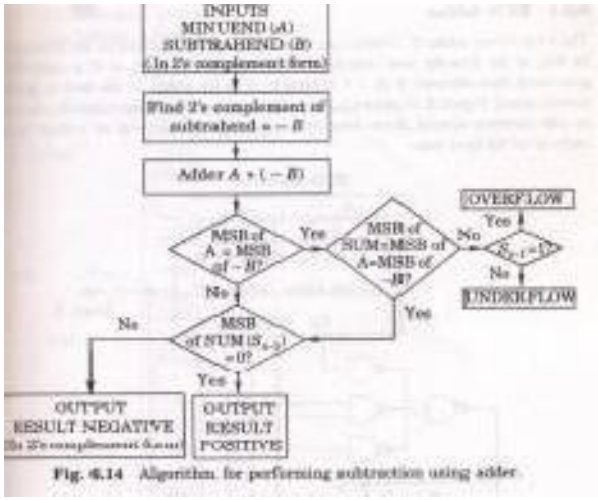


Fig. 6.14 Algorithm for performing subtraction using adder

Fig 7.18a: Algorithm to perform subtraction using adder

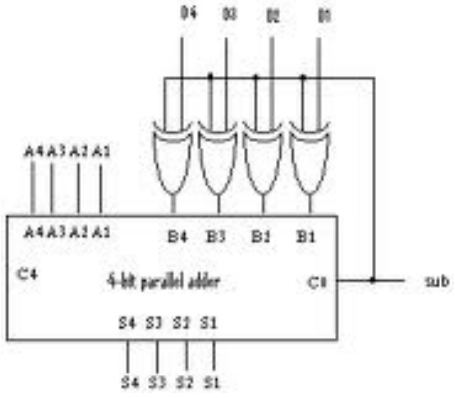


Fig 7.18b: Logic circuit for performing subtraction using adder

DIGITAL MAGNITUDE COMPARATOR

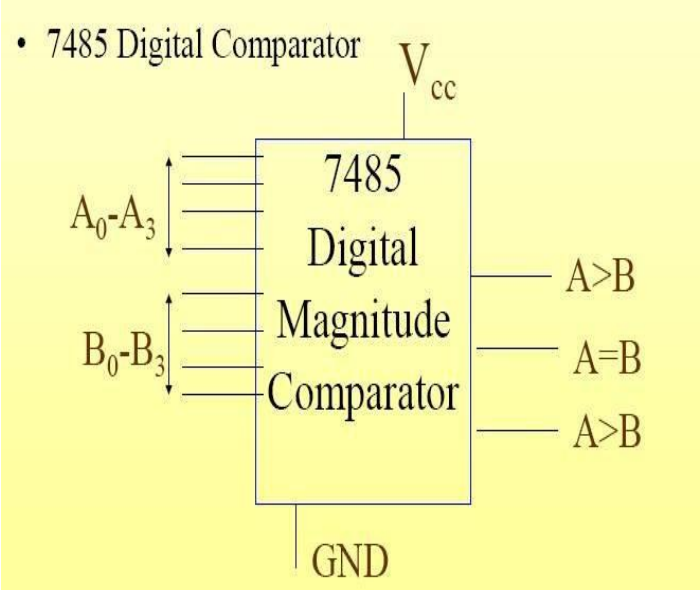


Fig 7.19 Logic symbol of IC 7485

Another common and very useful combinational logic circuit is that of the **Digital Comparator** circuit. Digital or Binary Comparators are made up from standard AND, NOR and NOT gates that compare the digital signals present at their input terminals and produce an output depending upon the condition of those inputs. For example, along with being able to add and subtract binary numbers we need to be able to compare them and determine whether the value of input A is greater than, smaller than or equal to the value at input B etc. The digital comparator accomplishes this using several logic gates that operate on the principles of Boolean algebra. There are two main types of digital comparator available and these are.

- Identity Comparator - is a digital comparator that has only one output terminal for when A = B either "HIGH" A = B = 1 or "LOW" A = B = 0
- Magnitude Comparator - is a type of digital comparator that has three output terminals, one each for equality, A = B greater than, A > B and less than A < B

The purpose of a **Digital Comparator** is to compare a set of variables or unknown numbers, for example A (A1, A2, A3, ... An, etc) against that of a constant or unknown value such as B (B1, B2, B3, Bn, etc) and produce an output condition or flag depending upon the result of the comparison. For example, a magnitude comparator of two 1-bits, (A and B) inputs would produce the following three output conditions when compared to each other.

$$A > B, \qquad A = B, \qquad A < B$$

Which means: A is greater than B, A is equal to B, and A is less than A

This is useful if we want to compare two variables and want to produce an output when any of the above three conditions are achieved. For example, produce an output from a counter when a certain count number is reached. Consider the simple 1-bit comparator in the fig 7.20 below.

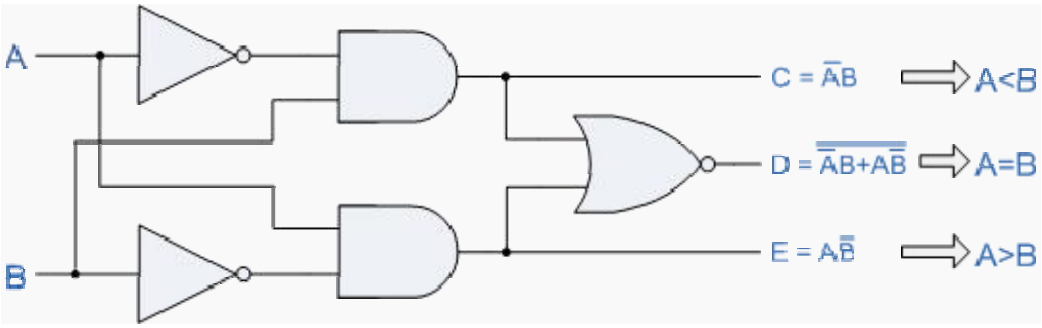


Fig 7.20: Logic circuit of 1-bit comparator

Then the operation of a 1-bit digital comparator is given in the following Truth Table 7.10

Inputs		Outputs		
B	A	A > B	A = B	A < B
0	0	0	1	0
0	1	1	0	0
1	0	0	0	1
1	1	0	1	0

Table 7.10: Truth Table of 1-bit comparator

You may notice two distinct features about the comparator from the above truth table. Firstly, the circuit does not distinguish between either two "0" or two "1"'s as an output A = B is produced when they are both equal, either A = B = "0" or A = B = "1". Secondly, the output condition for A = B resembles that of a commonly available logic gate, the Exclusive-NOR or Ex-NOR function (equivalence) on each of the n-bits giving: Q = A $\bigoplus$ B

Digital comparators actually use Exclusive-NOR gates within their design for comparing their respective pairs of bits. When we are comparing two binary or BCD values or variables against each other, we are comparing the "magnitude" of these values, a logic "0" against a logic "1" which is where the term **Magnitude Comparator** comes from.

As well as comparing individual bits, we can design larger bit comparators by cascading together n of these and produce a n-bit comparator just as we did for the n-bit adder in the previous tutorial. Multi-bit comparators can be constructed to compare whole binary or BCD words to produce an output if one word is larger, equal to or less than the other. A very good example of this is the 4-bit magnitude comparator. Here, two 4-bit words ("nibbles") are compared to each other to produce the relevant output with one word connected to inputs A and the other to be compared against connected to input B as shown below in fig 7.21.

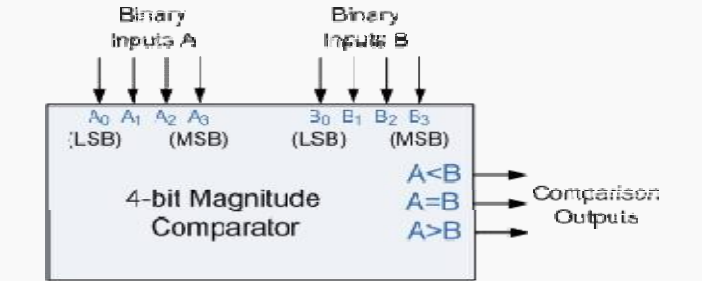


Fig 7.21: 4-bit magnitude comparator

Some commercially available digital comparators such as the TTL 7485 or CMOS 4063 4-bit magnitude comparator have additional input terminals that allow more individual comparators to be "cascaded" together to compare words larger than 4-bits with magnitude comparators of "n"-bits being produced. These cascading inputs are connected directly to the corresponding outputs of the previous comparator as shown to compare 8, 16 or even 32-bit words.

8-bit Word Comparator

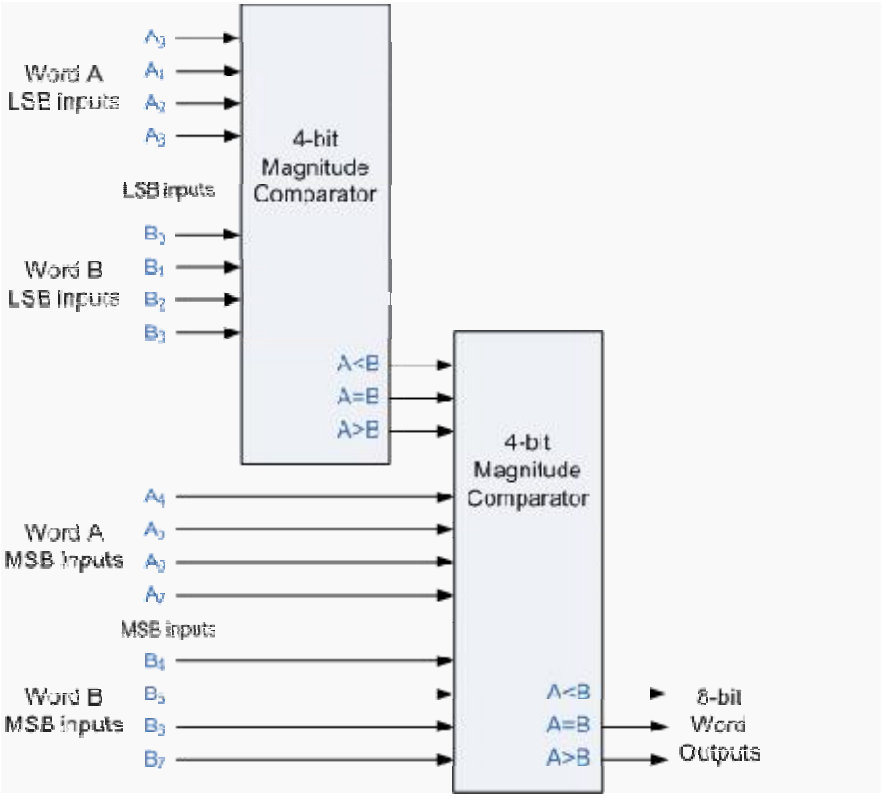


Fig 4.22: Two 4-bit comparators used to compare 8-bit number

When comparing large binary or BCD numbers like the example above, to save time the comparator starts by comparing the highest-order bit (MSB) first. If equality exists, A = B then it compares the next lowest bit and so on until it reaches the lowest-order bit, (LSB). If equality

still exists then the two numbers are defined as being equal. If inequality is found, either A > B or A < B the relationship between the two numbers is determined and the comparison between any additional lower order bits stops. **Digital Comparator**is used widely in Analogue-to-Digital converters, (ADC) and Arithmetic Logic Units, (ALU) to perform a variety of arithmetic operations.

SEQUENTIAL LOGIC BASICS

In digital circuit theory, **sequential logic** is a type of logic circuit whose output depends not only on the present value of its input signals but on the past history of its inputs. This is in contrast to *combinational logic*, whose output is a function of only the present input. That is, sequential logic has *state* (*memory*) while combinational logic does not. Or, in other words, sequential logic is combinational logic with memory as shown in the block diagram of fig8.1.

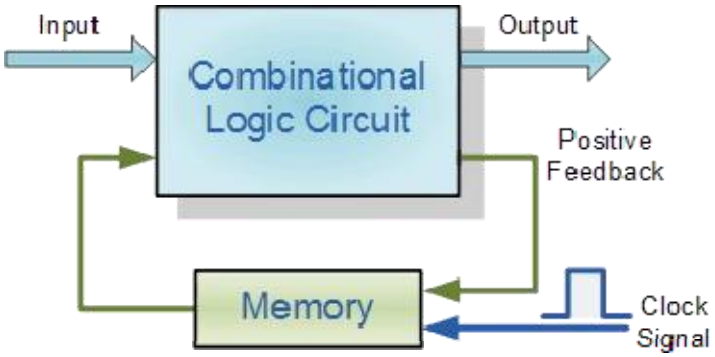


Fig 8.1 Sequential Logic Block diagram:

Sequential logic is used to construct finite state machines, a basic building block in all digital circuitry, as well as memory circuits and other devices. Virtually all circuits in practical digital devices are a mixture of combinational and sequential logic.

Digital sequential logic circuits are divided into synchronous and asynchronous types. In synchronous sequential circuits, the state of the device changes only at discrete times in response to a clock signal. In asynchronous circuits the state of the device can change at any time in response to changing inputs.

The word "Sequential" means that things happen in a "sequence", one after another and in **Sequential Logic** circuits, the actual clock signal determines when things will happen next. Simple sequential logic circuits can be constructed from standard **Bistable** circuits such as Flip-flops, Latches and Counters and which themselves can be made by simply connecting together universal *NAND Gates* and/or *NOR Gates* in a particular combinational way to produce the required sequential circuit.

SR FLIP-FLOP

The SR flip-flop can be considered as one of the most basic sequential logic circuit possible. The flip-flop is basically a one-bit memory bistable device that has two inputs, one which will "SET" the device (meaning the output = "1"), and is labelledS and another which will "RESET" the device (meaning the output = "0"), labelledR. Then the SR description stands for set/reset. The reset input resets the flip-flop back to its original state with an output Q that will be either at a logic level "1" or logic "0" depending upon this set/reset condition.

A basic NAND gate SR flip-flop circuit provides feedback from both of its outputs back to its inputs and is commonly used in memory circuits to store data bits. Then the SR flip-flop actually has three inputs, Set, Reset and its current output Q relating to its current state or history. The term "Flip-flop" relates to the actual operation of the device, as it can be "flipped" into one logic state or "flopped" back into another.

The NAND Gate SR Flip-Flop

The simplest way to make any basic one-bit set/reset SR flip-flop is to connect together a pair of cross-coupled 2-input NAND gates to form a set-reset bistable or an active LOW SR NAND Gate Latch, so that there is feedback from each output to one of the other NAND gate inputs. This device consists of two inputs, one called the *set*, S and the other called the *reset*, R with two corresponding outputs Q and its inverse or complement Q as shown in fig 8.2.

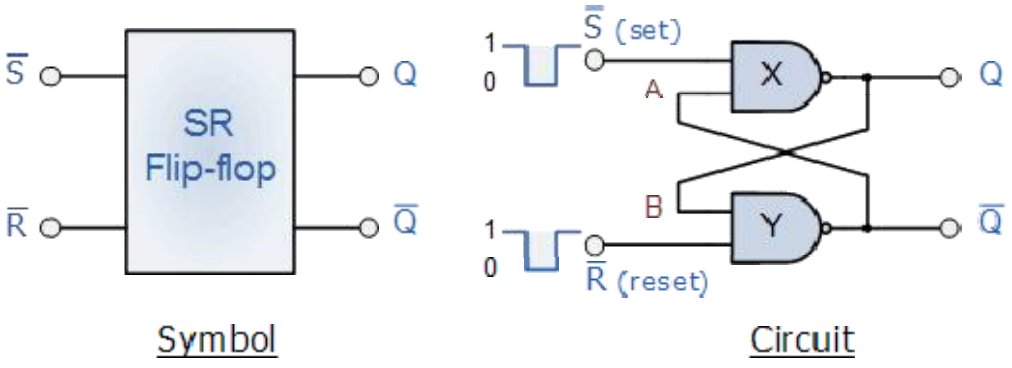


Fig 8.2 Nand gate SR flipflop

The Set State

Consider the circuit shown in the fig 2. If the input R is at logic level "0" (R = 0) and input S is at logic level "1" (S = 1), the NAND gate *Y* has at least one of its inputs at logic "0" therefore, its output Q must be at a logic level "1" (NAND Gate principles). Output Q is also fed back to input "A" and so both inputs to NAND gate *X* are at logic level "1", and therefore its output Q must be at logic level "0". Again NAND gate principals. If the reset input R changes state, and goes HIGH to logic "1" with S remaining HIGH also at logic level "1", NAND gate *Y* inputs are now R = "1" and B = "0". Since one of its inputs is still at logic level "0" the output at Q still remains HIGH at logic level "1" and there is no change of state. Therefore, the flip-flop circuit is said to be "Latched" or "Set" with Q = "1" and Q = "0".

Reset State

In this second stable state, Q is at logic level "0", not Q = "0" its inverse output Q is at logic level "1", Q = "1", and is given by R = "1" and S = "0". As gate *X* has one of its inputs at logic "0" its output Q must equal logic level "1" (again NAND gate principles). Output Q is fed back to input "B", so both inputs to NAND gate *Y* are at logic "1", therefore, Q = "0". If the set input, S now changes state to logic "1" with input R remaining at logic "1", output Q still remains LOW at logic level "0" and there is no change of state. Therefore, the flip-flop circuits "Reset" state has been latched. We can define this "set/reset" action in the following truth table 8.1.

State	S	R	Q	Q̄	Description
Set	1	0	1	0	Set Q » 1
	1	1	1	0	no change
Reset	0	1	0	1	Reset Q » 0
	1	1	0	1	no change
Invalid	0	0	0	1	memory with Q = 0
	0	0	1	0	memory with Q = 1

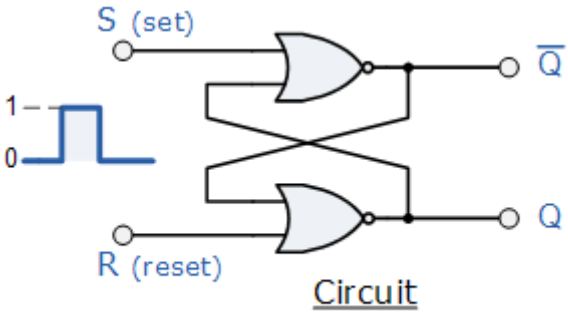
Table 8.1: Truth Table for this Set-Reset Function

It can be seen that when both inputs S = "1" and R = "1" the outputs Q and Q can be at either logic level "1" or "0", depending upon the state of inputs Sor R BEFORE this input condition existed. However, input state R = "0" and S = "0" is an undesirable or invalid condition and must be avoided because this will give both outputs Q and Q to be at logic level "1" at the same time and we would normally want Q to be the inverse of Q. However, if the two inputs are now switched HIGH again after this condition to logic "1", both the outputs will go LOW resulting in the flip-flop becoming unstable and switch to an unknown data state based upon the unbalance. This unbalance can cause one of the outputs to switch faster than the other resulting in the flip-flop switching to one state or the other which may not be the required state and data corruption will exist. This unstable condition is known as its **Meta-stable** state.

Then, a bistable SR flip-flop or SR latch is activated or set by a logic "1" applied to its S input and deactivated or reset by a logic "1" applied to its R. The SR flip-flop is said to be in an

"invalid" condition (Meta-stable) if both the set and reset inputs are activated simultaneously.

As well as using NAND gates, it is also possible to construct simple one-bit **SR Flip-flops** using two cross-coupled NOR gates connected in the same configuration. The circuit will



S	R	Q	$\overline{Q}$
0	0	No change	
0	1	0	1
1	0	1	0
1	1	0	0
		(Invalid)	

Fig 8.3 Nor gate SR flipflop

work in a similar way to the NAND gate circuit above, except that the inputs are active HIGH and the invalid condition exists when both its inputs are at logic level "1" and this is shown below in fig 8.3.

Gated or Clocked SR Flip-Flop

It is sometimes desirable in sequential logic circuits to have a bistable SR flip-flop that only changes state when certain conditions are met regardless of the condition of either the Set or the Reset inputs. By connecting a 2-input AND gate in series with each input terminal of the SR Flip-flop a Gated SR Flip-flop can be created. This extra conditional input is called an "Enable" input and is given the prefix of "EN". The addition of this input means that the output at Q only changes state when it is HIGH and can therefore be used as a clock (CLK) input making it level-sensitive as shown in fig 4.

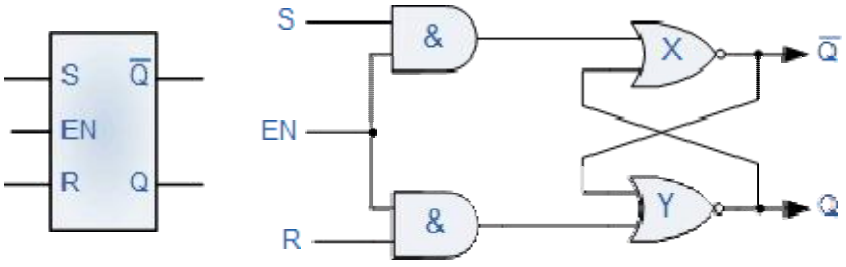


Fig 8.4 Clocked SR flipflop

When the Enable input "EN" is at logic level "0", the outputs of the two AND gates are also at logic level "0", (AND Gate principles) regardless of the condition of the two inputs S and R, latching the two outputs Q and Q into their last known state. When the enable input "EN" changes to logic level "1" the circuit responds as a normal SR bistable flip-flop with the two AND gates becoming transparent to the Set and Reset signals. This enable input can also be connected to a clock timing signal adding clock synchronisation to the flip-flop creating what is sometimes called a "Clocked SR Flip-flop". So a **Gated Bistable SR Flip-flop** operates as a

standard bistable latch but the outputs are only activated when a logic "1" is applied to its EN input and deactivated by a logic "0".

JK FLIP-FLOP

A basic gated SR NAND flip-flop suffers from two basic problems: number one, the S = 0 and R = 0 condition or S = R = 0 must always be avoided, and number two, if S or R change state while the enable input is high the correct latching action may not occur. Then to overcome these two fundamental design problems with the SR flip-flop, the **JK flip-Flop** was developed.

The **JK flip-Flop** is the most widely used of all the flip-flop designs and is considered to be a universal flip-flop circuit. The sequential operation of the JK flip-flop is exactly the same as for the previous SR flip-flop with the same "set" and "reset" inputs. The difference this time is that the JK flip-flop has no invalid or forbidden input states of the SR Latch (when S and R are both 1).

The **JK flip-flop** is basically a gated SR flip-flop with the addition of a clock input circuitry that prevents the illegal or invalid output condition that can occur when both inputs S and R are equal to logic level "1". Due to this additional clocked input, a JK flip-flop has four possible input combinations, "logic 1", "logic 0", "no change" and "toggle". The symbol for a JK flip-flop is similar to that of an *SR Bistable Latch* except for the addition of a clock input.

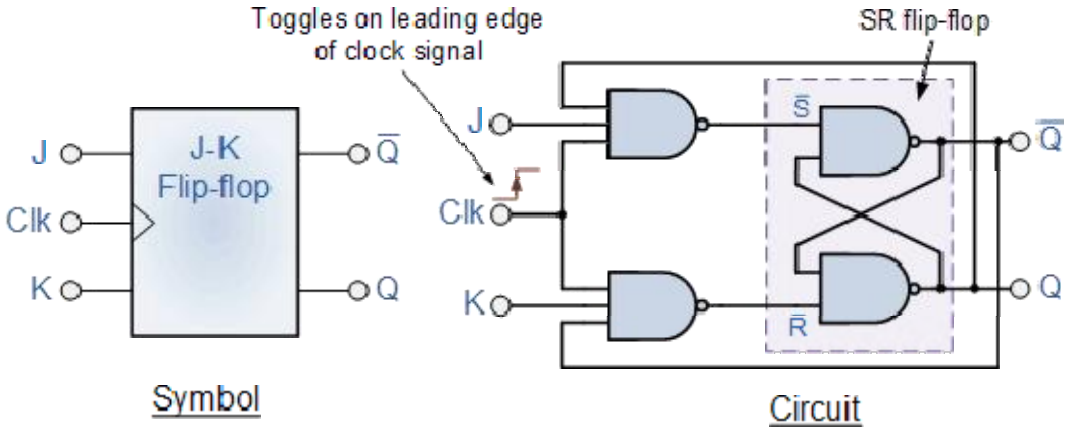


Fig 8.5 The Basic JK Flip-flop

The basic JK flip flop is shown in the fig 8.5. Both the S and the R inputs of the previous SR bistable have now been replaced by two inputs called the J and K inputs, respectively after its inventor Jack Kilby. Then this equates to: J = S and K = R.

The two 2-input AND gates of the gated SR bistable have now been replaced by two 3-

	J	K	Q	$\bar{Q}$	Description
same as for the SR Latch	0	0	0	0	Memory no change
	0	0	0	1	
	0	1	1	0	Reset Q » 0
	0	1	0	1	
	1	0	0	1	Set Q » 1
	1	0	1	0	
toggle action	1	1	0	1	Toggle
	1	1	1	0	

Table 8.2:Truth Table for the JK Function

input NAND gates with the third input of each gate connected to the outputs at Q and Q. This cross coupling of the SR flip-flop allows the previously invalid condition of S = "1" and R = "1" state to be used to produce a "toggle action" as the two inputs are now interlocked. If the circuit is "SET" the J input is inhibited by the "0" status of Q through the lower NAND gate. If the circuit is “RESET” the K input is inhibited by the "0" status of Q through the upper NAND gate As Q and Q are always different we can use them to control the input. When both inputs J and K are equal to logic "1", the JK flip-flop toggles as shown in the following truth table 8.2.Then the JK flip-flop is basically an SR flip-flop with feedback which enables only one of its two input terminals, either SET or RESET to be active at any one time thereby eliminating the invalid condition seen previously in the SR flip-flop circuit. Also when both the J and the K inputs are at logic level "1" at the same time, and the clock input is pulsed either "HIGH", the circuit will "toggle" from its SET state to a RESET state, or visa-versa. This results in the JK flip-flop acting more like a T-type toggle flip-flop when both terminals are HIGH.

Although this circuit is an improvement on the clocked SR flip-flop it still suffers from timing problems called "race" if the output Q changes state before the timing pulse of the clock input has time to go "OFF". To avoid this the timing pulse period (T) must be kept as short as possible (high frequency). As this is sometimes not possible with modern TTL IC's the much improved **Master-Slave JK Flip-flop** was developed. This eliminates all the timing problems by using two SR flip-flops connected together in series, one for the "Master" circuit, which triggers on the leading edge of the clock pulse and the other, the "Slave" circuit, which triggers on the falling edge of the clock pulse. This results in the two sections, the master section and the slave section being enabled during opposite half-cycles of the clock signal.

Dual JK Flip-flop 74LS73

The 74LS73 is a Dual JK flip-flop IC shown in fig 8.6, which contains two individual JK

type bistable's within a single chip enabling single or master-slave toggle flip-flops to be made.

Other JK flip-flop IC's include the 74LS107 Dual JK flip-flop with clear, the 74LS109 Dual positive-edge triggered JK flip-flop and the 74LS112 Dual negative-edge triggered flip-flop with

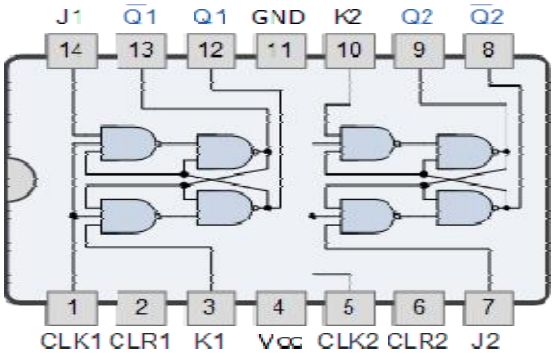


Fig 8.6 Dual JK Flip-flop 74LS73

both preset and clear inputs

The Master-Slave JK Flip-flop

The **Master-Slave Flip-Flop** is basically two gated SR flip-flops connected together in a series configuration with the slave having an inverted clock pulse. The outputs from Q and Q from the "Slave" flip-flop are fed back to the inputs of the "Master" with the outputs of the "Master" flip-flop being connected to the two inputs of the "Slave" flip-flop. This feedback configuration from the slave's output to the master's input gives the characteristic toggle of the JK flip-flop as shown fig 8.7.

The input signals J and K are connected to the gated "master" SR flip-flop which "locks" the input condition while the clock (Clk) input is "HIGH" at logic level "1". As the clock input of the "slave" flip-flop is the inverse (complement) of the "master" clock input, the "slave" SR flip-flop does not toggle. The outputs from the "master" flip-flop are only "seen" by the gated "slave" flip-flop when the clock input goes "LOW" to logic level "0". When the clock is "LOW", the outputs from the "master" flip-flop are latched and any additional changes to its inputs are ignored. The gated "slave" flip-flop now responds to the state of its inputs passed over by the "master" section. Then on the "Low-to-High" transition of the clock pulse the inputs of the "master" flip-flop are fed through to the gated inputs of the "slave" flip-flop and on the "High-to-Low" transition the same inputs are reflected on the output of the "slave" making this type of flip-flop edge or pulse-triggered.

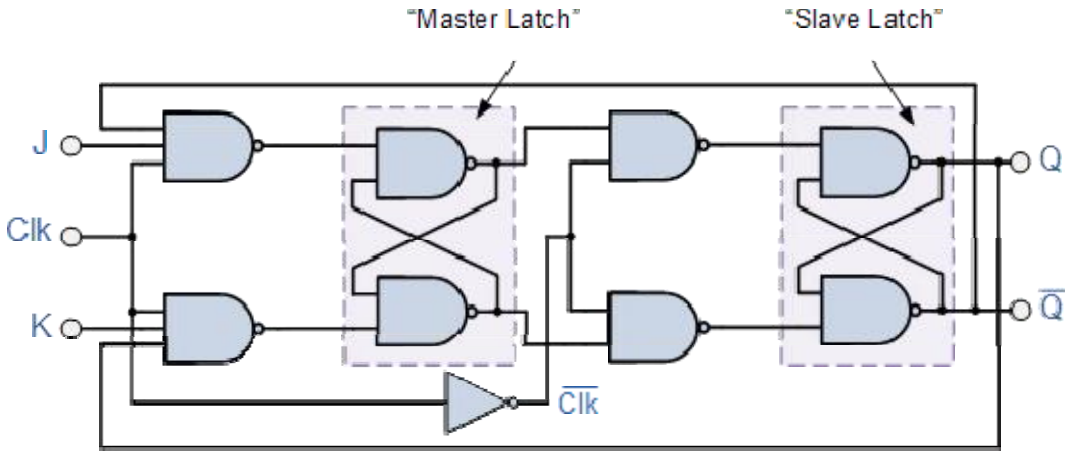


Fig 8.7 The Master-Slave JK Flip-Flop

Then, the circuit accepts input data when the clock signal is "HIGH", and passes the data to the output on the falling-edge of the clock signal. In other words, the **Master-Slave JK Flip-flop** is a "Synchronous" device as it only passes data with the timing of the clock signal.

D FLIP-FLOP

One of the main disadvantages of the basic *SR NAND Gate*bistable circuit is that the indeterminate input condition of "SET" = logic "0" and "RESET" = logic "0" is forbidden. This state will force both outputs to be at logic "1", over-riding the feedback latching action and whichever input goes to logic level "1" first will lose control, while the other input still at logic "0" controls the resulting state of the latch. In order to prevent this from happening an inverter can be connected between the "SET" and the "RESET" inputs to produce another type of flip-flop circuit called a **Data Latch**, **Delay flip-flop**, **D-type Bistable** or simply a **D-type flip-flop** as it is more generally called.

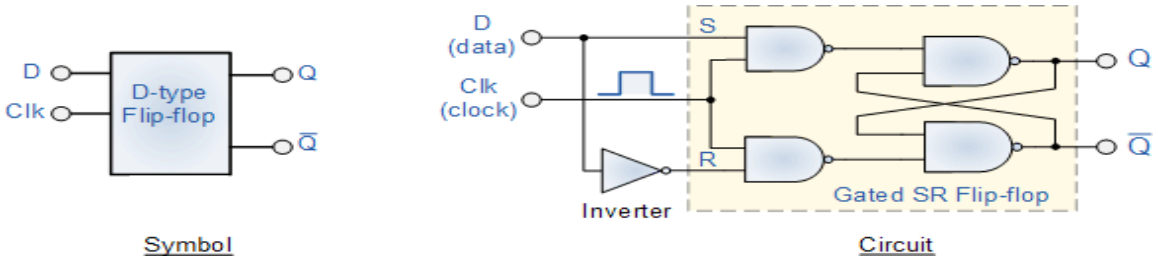


Fig 8.8 Symbol and Logic circuit of D flip-flop

The **D flip-flop** is by far the most important of the clocked flip-flops as it ensures that ensures that inputs S and R are never equal to one at the same time. D-type flip-flops are constructed from a gated SR flip-flop with an inverter added between the S and the R inputs to allow for a single D (data) input. This single data input D is used in place of the "set" signal, and the inverter is used to generate the complementary "reset" input thereby making a level-sensitive D-type flip-flop from a level-sensitive RS-latch as now S = D and R = not D as shown in fig 8.8.

We remember that a simple SR flip-flop requires two inputs, one to "SET" the output and one to "RESET" the output. By connecting an inverter (NOT gate) to the SR flip-flop we can "SET" and "RESET" the flip-flop using just one input as now the two input signals are complements of each other. This complement avoids the ambiguity inherent in the SR latch when both inputs are LOW, since that state is no longer possible.

Thus the single input is called the "DATA" input. If this data input is HIGH the flip-flop would be "SET" and when it is LOW the flip-flop would be "RESET". However, this would be rather pointless since the flip-flop's output would always change on every data input. To avoid this an additional input called the "CLOCK" or "ENABLE" input is used to isolate the data input from the flip-flop after the desired data has been stored. The effect is that D is only copied to the output Q when the clock is active. This then forms the basis of a **D flip-flop**.

Clk	D	Q	Q	Description
↓ » 0	X	Q	Q	Memory no change
↑ » 1	0	0	1	Reset Q » 0
↑ » 1	1	1	0	Set Q » 1

Table 8.3: Truth Table for the D Flip-flop

The **D flip-flop** will store and output whatever logic level is applied to its data terminal so long as the clock input is HIGH. Once the clock input goes LOW the "set" and "reset" inputs of the flip-flop are both held at logic level "1" so it will not change state and store whatever data was present on its output before the clock transition occurred. In other words the output is "latched" at either logic "0" or logic "1". The truth table is shown in table 8.3.

The Master-Slave D Flip-flop

The basic **D flip-flop** can be improved further by adding a second SR flip-flop to its output that is activated on the complementary clock signal to produce a "Master-Slave D flip-flop". On the leading edge of the clock signal (LOW-to-HIGH) the first stage, the "master" latches the input condition at D, while the output stage is deactivated. On the trailing edge of the clock signal (HIGH-to-LOW) the second "slave" stage is now activated, latching on to the output from the first master circuit. Then the output stage appears to be triggered on the negative edge of the clock pulse. "Master-Slave D flip-flops" can be constructed by the cascading together of two latches with opposite clock phases as shown in fig 8.9.

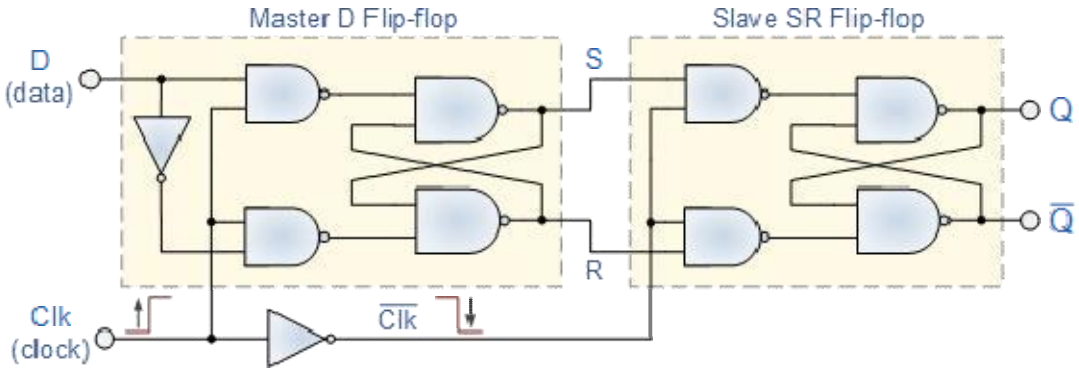


Fig 8.9 Master-Slave D flip-flop Circuit

We can see from above that on the leading edge of the clock pulse the master flip-flop will be loading data from the data D input, therefore the master is "ON". With the trailing edge of the clock pulse the slave flip-flop is loading data, i.e. the slave is "ON". Then there will always be one flip-flop "ON" and the other "OFF" but never both the master and slave "ON" at the same time. Therefore, the output Q acquires the value of D, only when one complete pulse, i.e. 0-1-0 is applied to the clock input.

There are many different D flip-flop IC's available in both TTL and CMOS packages with the more common being the 74LS74 (fig 8.10) which is a Dual D flip-flop IC, which contains two individual D type bistable's within a single chip enabling single or master-slave toggle flip-flops to be made. Other D flip-flop IC's include the 74LS174 HEX D flip-flop with direct clear input, the 74LS175 Quad D flip-flop with complementary outputs and the 74LS273 Octal D flip-flop containing eight D flip-flops with a clear input in one single package.

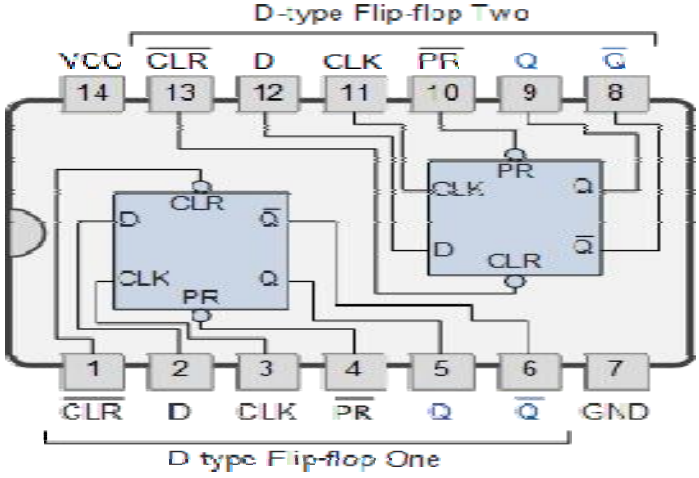


Fig 8.10 Dual D flip-flop 74LS74

APPLICATIONS OF D_FLIPFLOP:

i) Frequency Division

One main use of a D flip-flop is as a ***Frequency Divider*.** If the Q output on a D-type flip-flop is connected directly to the D input giving the device closed loop "feedback", successive clock pulses will make the bistable "toggle" once every two clock cycles.

In the counters tutorials we saw how the **Data Latch** can be used as a "Binary Divider", or a "Frequency Divider" to produce a "divide-by-2" counter circuit, that is, the output has half the

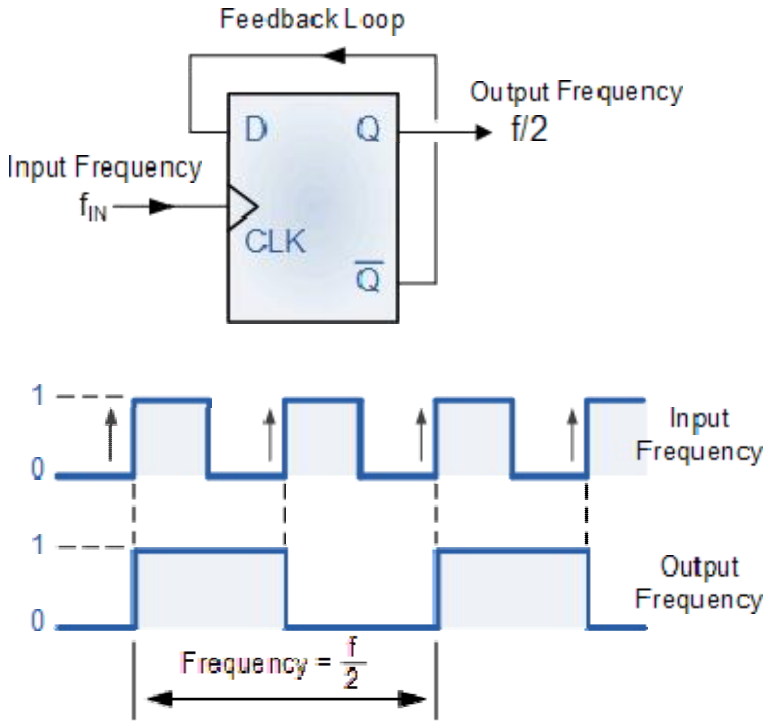


Fig 8.11 Divide-by-2 Counter

frequency of the clock pulses. By placing a feedback loop around the D flip-flop another type of flip-flop circuit can be constructed called a **T-type flip-flop** or more commonly a T-type bistable, that can be used as a divide-by-two circuit in binary counters as shown below in fig 8.11.

It can be seen from the frequency waveforms above, that by "feeding back" the output from Q to the input terminal D, the output pulses at Q have a frequency that are exactly one half (f/2) that of the input clock frequency, (F_{in}). In other words the circuit produces **frequency division** as it now divides the input frequency by a factor of two (an octave) as Q = 1 once every two clock cycles.

ii) Data Latches

Another useful application of the Data Latch is to hold or remember the data present on its data input, thereby acting as a single bit memory device and IC's such as the TTL 74LS74 or the CMOS 4042 are available in Quad format for this purpose. By connecting together four, *1-bit* data latches so that all their clock terminals are connected at the same time a simple "4-bit" Data latch can be made as shown below in fig 8.12.

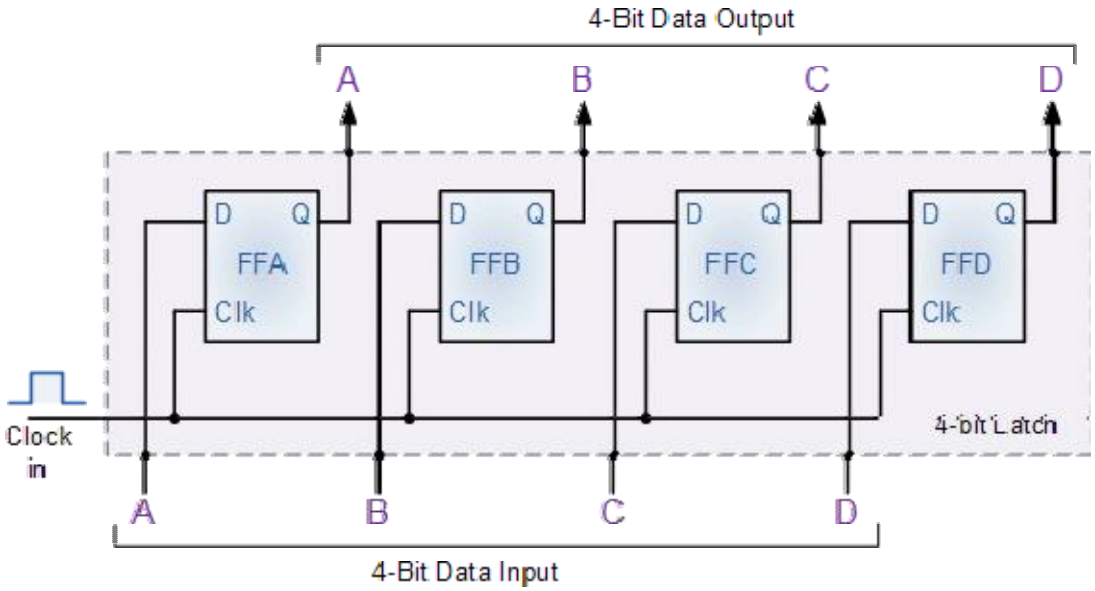


Fig 8.12: 4-bit Data Latch

The Data Latch is a very useful device in electronic and computer circuits. They can be designed to have very high output impedance at both outputs Q and its inverse or complement output Q to reduce the impedance effect on the connecting circuit when used as a buffer, I/O port, bi-directional bus driver or even a display driver. But a single "1-bit" data latch is not very practical to use on its own and instead commercially available IC's incorporate 4, 8, 10, 16 or even 32 individual data latches into one single IC package, and one such IC device is the 74LS373 Octal D-type transparent latch.

D flip-flop Summary

The data or **D flip-flop** can be built from a pair of back-to-back latches by connecting an inverter between the S and the R inputs to allow for a single D (data) input. The basic D-type flip-flop circuit can be improved further by adding a second SR flip-flop to its output that is activated on the complementary clock signal to produce a "Master-Slave D flip-flop". The difference between a D-type latch and a D flip-flop is that a latch does not have a clock signal, whereas a flip-flop always does. The D flip-flop is an edge triggered device which transfers input data to Q on clock rising or falling edge. Data Latches are Level sensitive devices such as the data latch and the transparent latch.

THE SHIFT REGISTER

The **Shift Register** is another type of sequential logic circuit that is used for the storage or transfer of data in the form of binary numbers and then "shifts" the data out once every clock

cycle, hence the name "shift register". It basically consists of several single bit "D-Type Data Latches", one for each bit (0 or 1) connected together in a serial or daisy-chain arrangement so that the output from one data latch becomes the input of the next latch and so on. The data bits may be fed in or out of the register serially, i.e. one after the other from either the left or the right direction, or in parallel, i.e. all together. The number of individual data latches required to make up a single **Shift Register** is determined by the number of bits to be stored with the most common being 8-bits wide, i.e. eight individual data latches.

The Shift Register is used for data storage or data movement and are used in calculators or computers to store data such as two binary numbers before they are added together, or to convert the data from either a serial to parallel or parallel to serial format. The individual data latches that make up a single shift register are all driven by a common clock (Clk) signal making them synchronous devices. Shift register IC's are generally provided with a *clear* or *reset* connection so that they can be "SET" or "RESET" as required.

Generally, shift registers operate in one of four different modes with the basic movement of data through a shift register being:

- Serial-in to Parallel-out (SIPO) - the register is loaded with serial data, one bit at a time, with the stored data being available in parallel form.
- Serial-in to Serial-out (SISO) - the data is shifted serially "IN" and "OUT" of the register, one bit at a time in either a left or right direction under clock control.
- Parallel-in to Serial-out (PISO) - the parallel data is loaded into the register simultaneously and is shifted out of the register serially one bit at a time under clock control.
- Parallel-in to Parallel-out (PIPO) - the parallel data is loaded simultaneously into the register, and transferred together to their respective outputs by the same clock pulse.

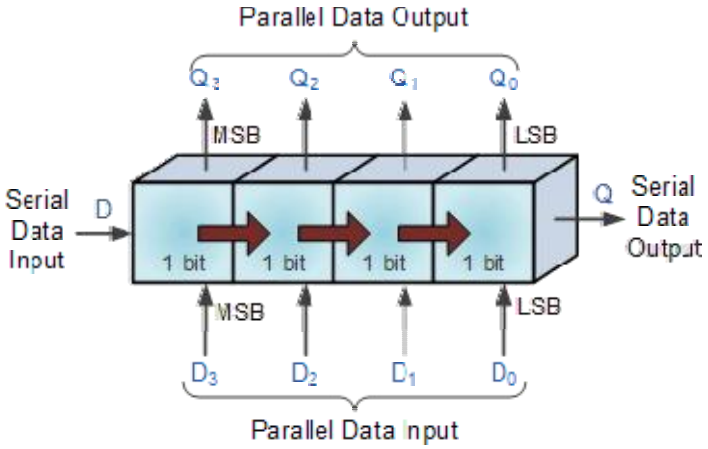


Fig 8.13 modes of operation of shift register

The effect of data movement from left to right through ashift register can be presented graphically as in fig 8.13:

Also, the directional movement of the data through a shift register can be either to the left, (left shifting) to the right, (right shifting) left-in but right-out, (rotation) or both left and right

shifting within the same register thereby making it *bidirectional*. It is assumed that all the data shifts to the right, (right shifting).

SERIAL-IN PARALLEL-OUT (SIPO)

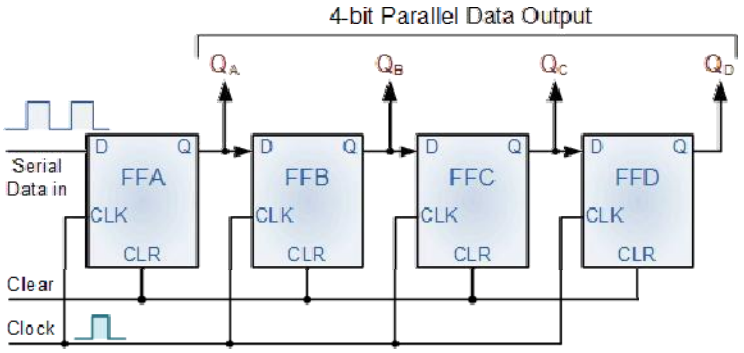


Fig 8.14 SIPO operation

The operation of fig 8.14 is as follows. Let's assume that all the flip-flops (**FFA** to **FFD**) have just been RESET (CLEAR input) and that all the outputs $\mathbf{Q_A}$ to $\mathbf{Q_D}$ are at logic level "0" i.e, no parallel data output. If a logic "1" is connected to the **DATA** input pin of **FFA** then on the first clock pulse the output of **FFA** and therefore the resulting $\mathbf{Q_A}$ will be set HIGH to logic "1" with all the other outputs still remaining LOW at logic "0". Assume now that the **DATA** input pin of **FFA** has returned LOW again to logic "0" giving us one data pulse or 0-1-0.

The second clock pulse will change the output of FFA to logic "0" and the output of FFB and Q_B HIGH to logic "1" as its input D has the logic "1" level on it from Q_A. The logic "1" has now moved or been "shifted" one place along the register to the right as it is now at Q_A. When the third clock pulse arrives this logic "1" value moves to the output of FFC (Q_C) and so on until the arrival of the fifth clock pulse which sets all the outputs Q_A to Q_D back again to logic level "0" because the input to FFA has remained constant at logic level "0".

The effect of each clock pulse is to shift the data contents of each stage one place to the right, and this is shown in the following table until the complete data value of 0-0-0-1 is stored in the register. This data value can now be read directly from the outputs of Q_A to Q_D. Then the data has been converted from a serial data input signal to a parallel data output. The truth table 8.3 and waveforms in fig 8.14a shows the propagation of the logic "1" through the register from left to right as follows.

Basic Movement of Data through a Shift Register

Clock Pulse No	QA	QB	QC	QD
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0

3	0	0	1	0

4	0	0	0	1
5	0	0	0	0

Table 8.3 SIPO Operation

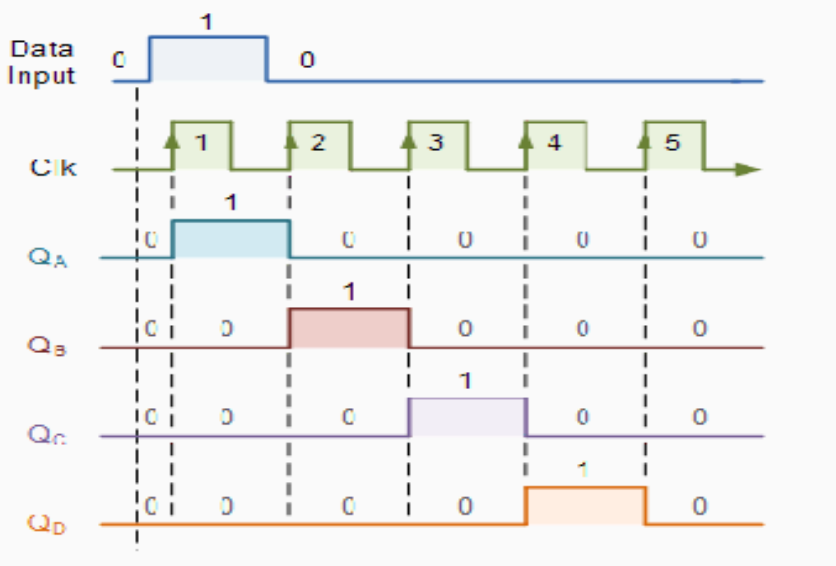


Fig 8.14a wave forms of Serial in parallel out operation

Note that after the fourth clock pulse has ended the 4-bits of data (0-0-0-1) are stored in the register and will remain there provided clocking of the register has stopped. In practice the input data to the register may consist of various combinations of logic "1" and "0". Commonly available SIPO IC's include the standard 8-bit 74LS164 or the 74LS594.

SERIAL-IN SERIAL-OUT (SISO)

This **shift register** is very similar to the SIPO above, except were before the data was read directly in a parallel form from the outputs Q_A to Q_D, this time the data is allowed to flow straight through the register and out of the other end. Since there is only one output, the DATA leaves the shift register one bit at a time in a serial pattern, hence the name **Serial-in to Serial-Out Shift Register** or **SISO**.

The SISO shift register (fig 8.15) is one of the simplest of the four configurations as it has only three connections, the serial input (SI) which determines what enters the left hand flip-flop, the serial output (SO) which is taken from the output of the right hand flip-flop and the

sequencing clock signal (Clk).

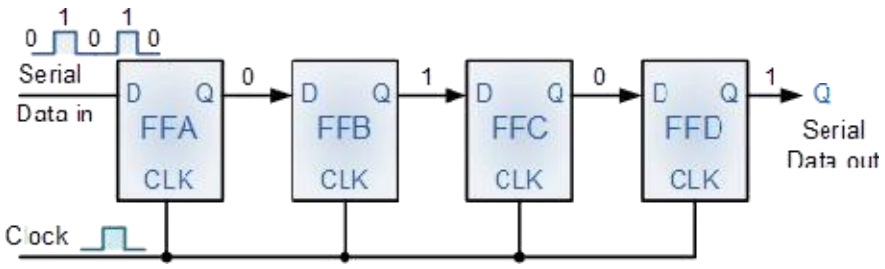


Fig 8.15: 4- bit SISO

This type of **Shift Register** also acts as a temporary storage device or as a time delay device for the data, with the amount of time delay being controlled by the number of stages in the register, 4, 8, 16 etc or by varying the application of the clock pulses. Commonly available IC's include the 74HC595 8-bit Serial-in/Serial-out Shift Register all with 3-state outputs.

PARALLEL-IN SERIAL-OUT (PISO)

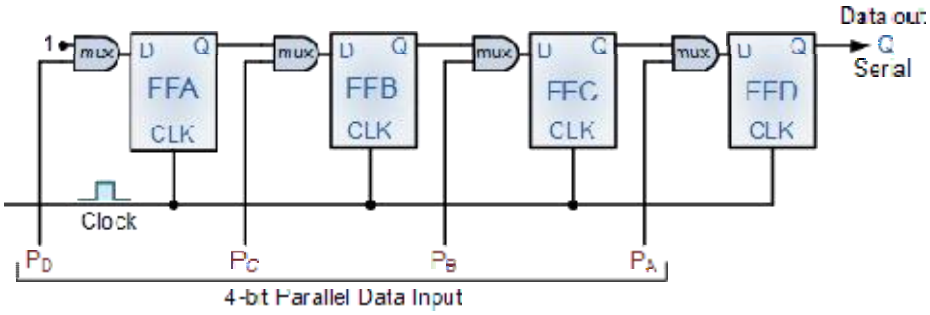


Fig 8.16: 4-bit Parallel-in to Serial-out Shift Register

The Parallel-in to Serial-out shift register (fig 8.16) acts in the opposite way to the serial-in to parallel-out one above. The data is loaded into the register in a parallel format i.e. all the data bits enter their inputs simultaneously, to the parallel input pins P_A to P_D of the register. The data is then read out sequentially in the normal shift-right mode from the register at Q representing thedata present at P_A to P_D. This data is outputted one bit at a time on each clock cycle in a serial format. It is important to note that with this system a clock pulse is not required to parallel load the register as it is already present, but four clock pulses are required to unload the data.

As this type of shift register converts parallel data, such as an 8-bit data word into serial format, it can be used to multiplex many different input lines into a single serial DATA stream which can be sent directly to a computer or transmitted over a communications line. Commonly available IC's include the 74HC166 8-bit Parallel-in/Serial-out Shift Registers.

PARALLEL-IN PARALLEL-OUT (PIPO)

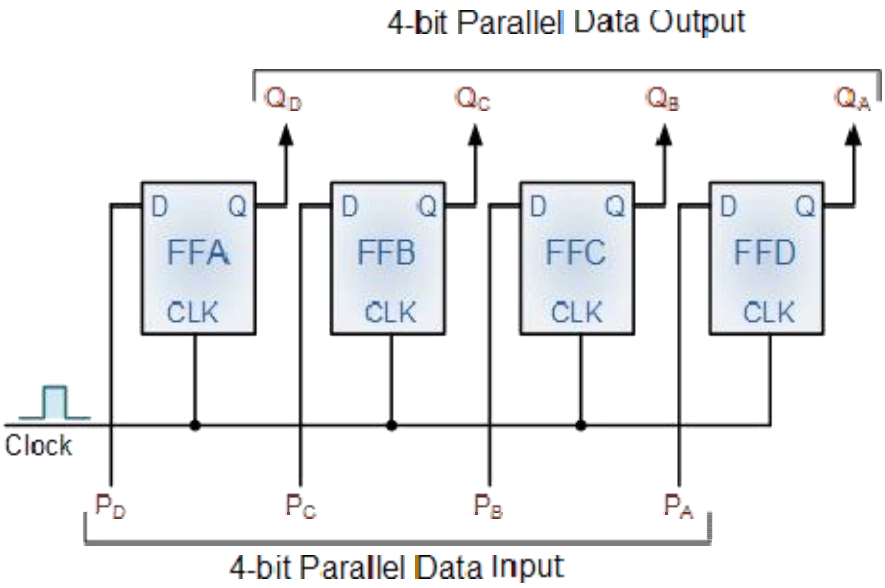


Fig 8.17: 4-bit Parallel-in to Parallel-out Shift Register

The final mode of operation is the Parallel-in to Parallel-out Shift Register (fig 8.17). This type of register also acts as a temporary storage device or as a time delay device similar to the SISO configuration above. The data is presented in a parallel format to the parallel input pins P_A to P_D and then transferred together directly to their respective output pins Q_A to Q_A by the same clock pulse. Then one clock pulse loads and unloads the register.

The PIPO shift register is the simplest of the four configurations as it has only three connections, the parallel input (PI) which determines what enters the flip-flop, the parallel output (PO) and the sequencing clock signal (Clk).

Similar to the Serial-in to Serial-out shift register, this type of register also acts as a temporary storage device or as a time delay device, with the amount of time delay being varied by the frequency of the clock pulses. Also, in this type of register there are no interconnections between the individual flip-flops since no serial shifting of the data is required.

UNIVERSAL SHIFT REGISTER

Today, high speed bi-directional "universal" type **Shift Registers** such as the TTL 74LS194, 74LS195 or the CMOS 4035 are available as a 4-bit multi-function devices that can be used in either serial-to-serial, left shifting, right shifting, serial-to-parallel, parallel-to-serial, and as a parallel-to-parallel multifunction data register, hence the name "Universal". These devices can perform any combination of parallel and serial input to output operations but require additional inputs to specify desired function and to pre-load and reset the device. The pin diagram is shown in fig 8.18.

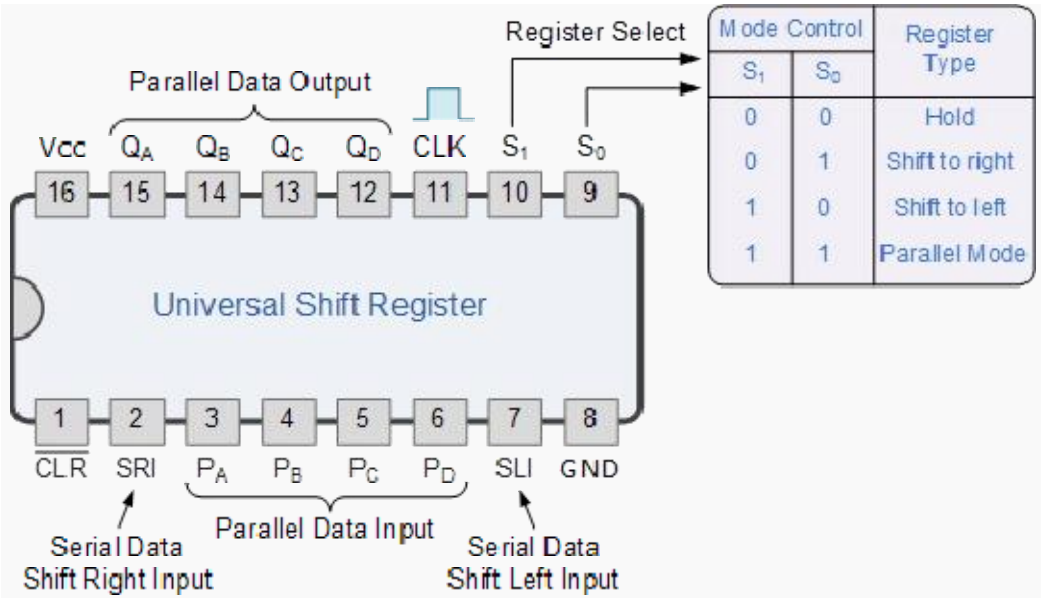


Fig 8.18: 4-bit Universal Shift Register 74LS194

Universal shift registers are very useful digital devices. They can be configured to respond to operations that require some form of temporary memory, delay information such as the SISO or PIPO configuration modes or transfer data from one point to another in either a serial or parallel format. Universal shift registers are frequently used in arithmetic operations to shift data to the left or right for multiplication or division.

Summary of Shift Registers

- A simple **Shift Register** can be made using only D-type flip-Flops, one flip-Flop for each data bit.
- The output from each flip-Flop is connected to the D input of the flip-flop at its right.
- Shift registers hold the data in their memory which is moved or "shifted" to their required positions on each clock pulse.
- Each clock pulse shifts the contents of the register one bit position to either the left or the right.
- The data bits can be loaded one bit at a time in a series input (SI) configuration or be loaded simultaneously in a parallel configuration (PI).
- Data may be removed from the register one bit at a time for a series output (SO) or removed all at the same time from a parallel output (PO).
- One application of shift registers is converting between serial and parallel data.
- Shift registers are identified as SIPO, SISO, PISO, PIPO, and universal shift registers.

APPLICATIONS OF SHIFT REGISTERS

The primary use of shift registers is temporary storage of data and bit manipulations. Some of the common applications are

i. Delay Line

A SISO register may be used to introduce time delay Δt in digital signals given by

$$\Delta t = N \times \frac{1}{f_c}$$

Where N is the number of stages and f_c is the clock frequency. Thus, an input pulse train appears at the output delayed by Δt. The amount of delay can be controlled by clock frequency or the number of FLIP-FLOPS in the shift register.

ii. Serial to parallel converter

Data in the serial form can be converted into parallel form by using a SIPO shift register.

iii. Parallel to Serial Converter

Data in the parallel form can be converted into serial form by using a PISO shift register

iv. Ring Counter

The synchronous **4-bitRing Counter**in the above fig 8.19 is preset so that exactly one data bit in the register is set to logic "1" with all the other bits reset to "0". To achieve this, a "CLEAR" signal is firstly applied to all the flip-flops together in order to "RESET" their outputs to a logic"0" level and then a "PRESET" pulse is applied to the input of the first flip-flop (FFA) before theclock pulses are applied. This then places a single logic "1" value into

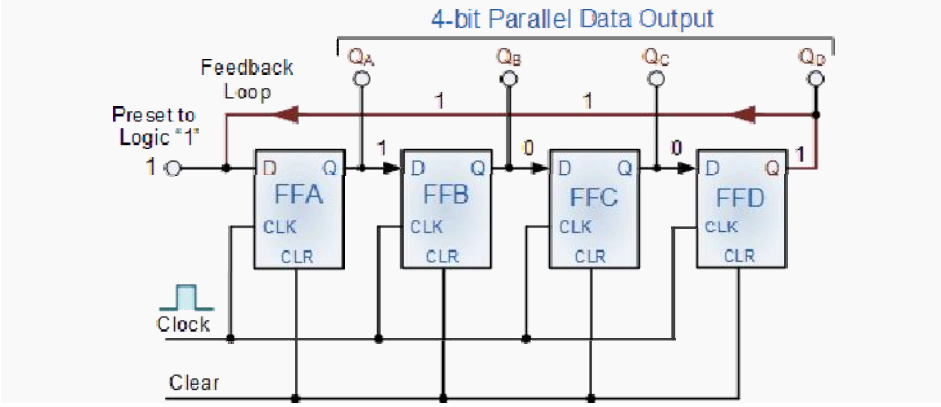


Fig 8.19: 4-bit Ring Counter

the circuit of the ring counter . On each successive clock pulse, the counter circulates the same data bit between the four flip-flops over and over again around the "ring" every fourth clock cycle. But in order to cycle the data correctly around the counter we must first "load" the counter

with a suitable data pattern as all logic "0"'s or all logic "1"'s outputted at each clock cycle would make the ring counter invalid.

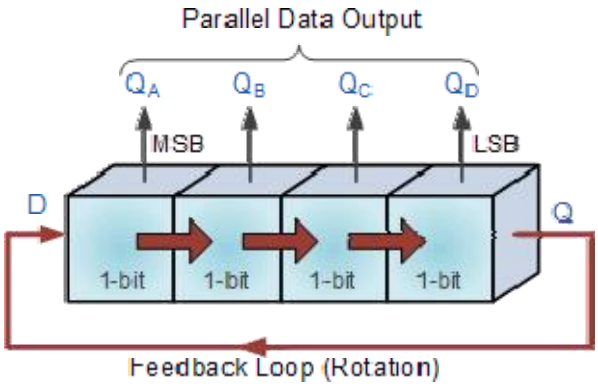


Fig 8.20a: Rotational Movement of a Ring Counter

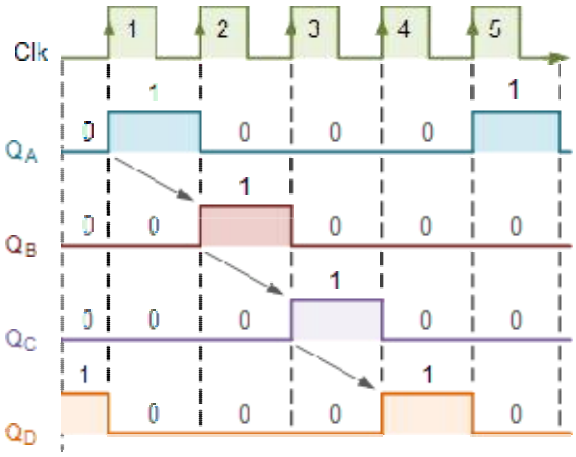


Fig 8.20b: Timing diagram

This type of data movement is called "rotation", and like the previous shift register, the effect of the movement of the data bit from left to right through a ring counter can be presented graphically as follows along with its timing diagram shown in fig 8.20(a & b):

Since the ring counter example shown above has four distinct states, it is also known as a "modulo-4" or "mod-4" counter with each flip-flop output having a frequency value equal to one-fourth or a quarter (1/4) that of the main clock frequency.

The "MODULO" or "MODULUS" of a counter is the number of states the counter counts or sequences through before repeating itself and a ring counter can be made to output any modulo number. A "mod-n" ring counter will require "n" number of flip-flops connected together to circulate a single data bit providing "n" different output states. For example, a mod-8 ring counter requires eight flip-flops and a mod-16 ring counter would require sixteen flip-flops. However, as in our example above, only four of the possible sixteen states are used, making ring counters very inefficient in terms of their output state usage.

v. Johnson Ring Counter

The **Johnson Ring Counter** or "Twisted Ring Counters", is another shift register with feedback exactly the same as the standard *Ring Counter* above, except that this time the inverted output Q of the last flip-flop is now connected back to the input D of the first flip-flop as shown below in fig 8.21. The main advantage of this type of ring counter is that it only needs half the number of flip-flops compared to the standard ring counter then its modulo number is halved. So a "n-stage" Johnson counter will circulate a single data bit giving sequence of 2n different states and can therefore be considered as a "mod-2n counter".

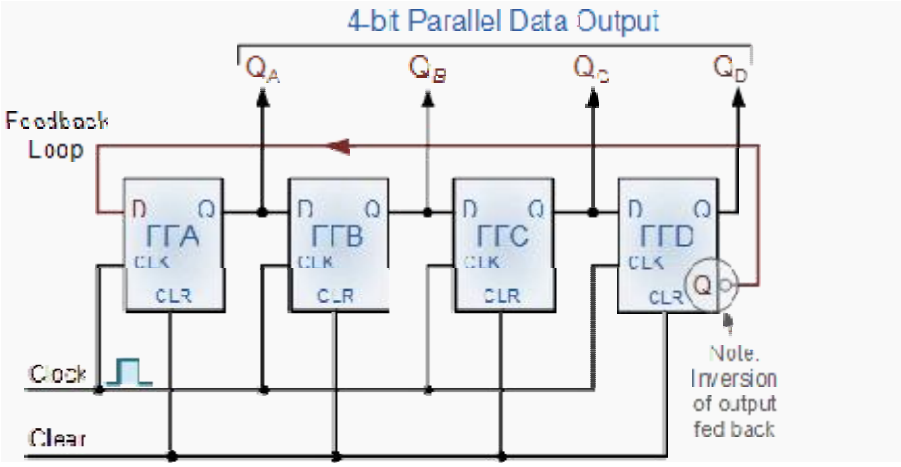


Fig 8.21: 4-bit Johnson Ring Counter

This inversion of Q before it is fed back to input D causes the counter to "count" in a different way. Instead of counting through a fixed set of patterns like the normal ring counter such as for a 4-bit counter, "0001"(1), "0010"(2), "0100"(4), "1000"(8) and repeat, the Johnson counter counts up and then down as the initial logic "1" passes through it to the right replacing the preceding logic "0". A 4-bit Johnson ring counter passes blocks of four logic"0" and then four logic "1" thereby producing an 8-bit pattern. As the inverted output Q is connected to the input D this 8-bit pattern continually repeats. For example, "1000", "1100", "1110", "1111", "0111", "0011", "0001", "0000" and this is demonstrated in the following table 8.4 below.

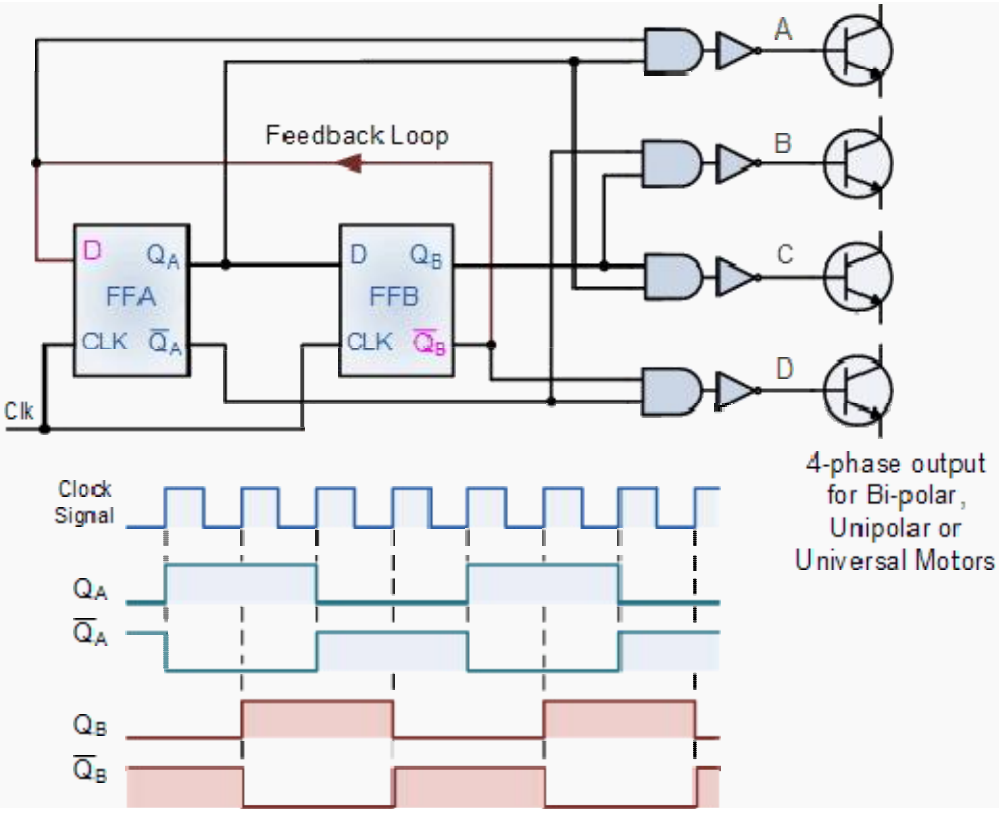
Clock Pulse No	FFA	FFB	FFC	FFD
0	0	0	0	0
1	1	0	0	0
2	1	1	0	0
3	1	1	1	0
4	1	1	1	1
5	0	1	1	1
6	0	0	1	1
7	0	0	0	1

Table8.4: Truth Table for a 4-bit Johnson Ring Counter

As well as counting or rotating data around a continuous loop, ring counters can also be used to detect or recognize various patterns or number values within a set of data. By connecting simple logic gates such as the *AND* or the *OR* gates to the outputs of the flip-flops the circuit can be made to detect a set number or value. Standard 2, 3 or 4-stage Johnson ring counters can also be used to divide the frequency of the clock signal by varying their feedback connections and divide-by-3 or divide-by-5 outputs are also available.

A 3-stage Johnson Ring Counter can also be used as a 3-phase, 120 degree phase shift square wave generator by connecting to the data outputs at A, B and NOT-B. The standard 5-stage Johnson counter such as the commonly available CD4017 is generally used as a synchronous decade counter/divider circuit. The smaller 2-stage circuit is also called a "Quadrature" (sine/cosine) Oscillator/Generator and is used to produce four individual outputs that are each "phase shifted" by 90 degrees with respect to each other, and this is shown below in fig 8.22.

2-bit Quadrature Generator



Output	A	B	C	D
Q_A+Q_B	1	0	0	0
Q_A+Q_B	0	1	0	0
Q_A+Q_B	0	0	1	0
Q_A+Q_B	0	0	0	1
2-bit Quadrature Oscillator, Count Sequence				

Fig 22: 2-bit Quadrature Generator

As the four outputs, A to D are phase shifted by 90 degrees with regards to each other, they can be used with additional circuitry, to drive a 2-phase full-step stepper motor for position control or the ability to rotate a motor to a particular location as shown in fig 8.23.

Stepper Motor Control

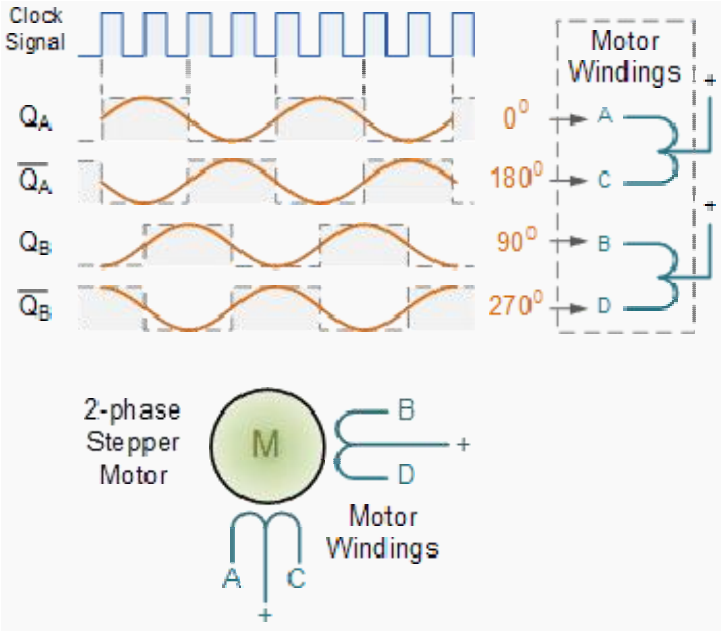


Fig 23: 2-phase (unipolar) Full-Step Stepper Motor Circuit

The speed of rotation of the *Stepper Motor* will depend mainly upon the clock frequency and additional circuitry would be require to drive the "power" requirements of the motor. As this section is only intended to give the reader a basic understanding of **Johnson Ring Counters** and its applications, other good websites explain in more detail the types and drive requirements of stepper motors.

Johnson Ring Counters are available in standard TTL or CMOS IC form, such as the

CD4017 5-Stage, decade Johnson ring counter with 10 active HIGH decoded outputs or the CD4022 4-stage, divide-by-8 Johnson counter with 8 active HIGH decoded outputs.

RIPPLE OR ASYNCHRONOUS COUNTER

A circuit used for counting the pulses s known as a counter. In previous section 5.7 two types of counters have been discussed. The number of states in an N stage ring counter is N, where as it is 2N in the case of moebius counter. These counters are referred to as modulo (or divided by N) and modulo 2N counters respectively, where modulo indicates the number of states in the counters. When the pulses to be counted are applied to a counter, it goes from state to state and the output of the flip-flops in the counter is decoded to read the count. The circuit comes back to its starting state after counting the N pulses in the case of modulo N counter.

The ring counter and the twisted ring counter do not make efficient use of flip-flops. A flip-flop has two states. Therefore a group of N flip-flops will have two 2^N states. This means it is possible to make a modulo 2^N counter using N flip-flops. Basically there are two types of such counters:

1. Asynchronous counter (Ripple counter)
2. Synchronous counter

In asynchronous counter, all the flip-flops are not clocked simultaneously, whereas in synchronous counter all the flip-flops are clocked simultaneously.

The available asynchronous ICs are given in the following table 8.5:

IC No.	**Description**
7490, 74290	BCD counter
7492	Divide by 12 counter
7493, 74293	4-bit binary counter
74176, 74196	Presettable BCD counter
74177, 74197	Presettable 4-bit binary counter
74390	Dual decade counter
74393	Dual 4 bit binary counter
74490	Dual BCD counter

Table 8.5

7490 RIPPLE COUNTER IC

The 7490 is a simple counter (fig 8.24), i.e. it can count from 0 to 9 cyclically in its natural mode. It counts the input pulses and the output is received as a 4-bit binary number through pins Q_A, Q_B, Q_C and Q_D. The binary output is reset to 0000 at every tenth pulse and count starts from 0 again. A pulse is also generated (probably at pin 9) as it resets its output to

0000. The chip can count up to other maximum numbers and return to zero by changing the modes of 7490. Thesemodes are set by changing the connection of reset pins R_1 - R_4.

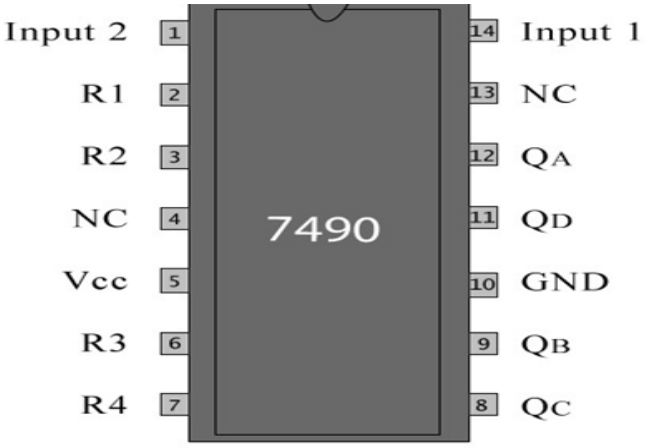
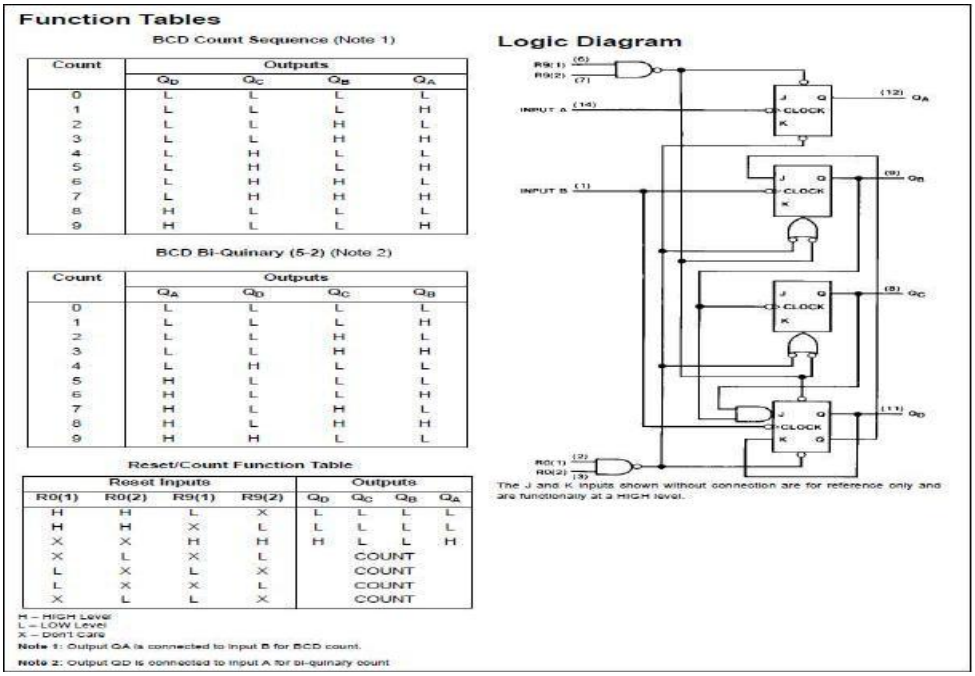


Fig 8.24: pin diagram of 7490

For example, if either R_1& R_2 are high or R_3& R_4 are ground, then it will reset Q_A, Q_B, Q_C and Q_D to 0. If resets R_3& R_4 are high, then the count on Q_A, Q_B, Q_C and Q_D goes to 1001.

The other high counts can be generated by connecting two or more 7490 ICs. For example, if two 7490 are connected in a manner that input of one becomes the output of other, the second IC will receive a pulse on every tenth count and will reset at every hundredth count. Thus this system can count from 0 to 99 and give corresponding BCD outputs.



Function Tables

BCD Count Sequence (Note 1)

Count	Outputs			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

BCD Bi-Quinary (5-2) (Note 2)

Count	Outputs			
	Q_A	Q_D	Q_C	Q_B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

Reset/Count Function Table

Reset Inputs				Outputs			
R0(1)	R0(2)	R9(1)	R9(2)	Q_D	Q_C	Q_B	Q_A
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
X	L	X	L	COUNT			
L	X	L	X	COUNT			
L	X	X	L	COUNT			
X	L	L	X	COUNT			

H – HIGH Level
L – LOW Level
X – Don't Care
Note 1: Output QA is connected to input B for BCD count.
Note 2: Output QD is connected to input A for bi-quinary count

Logic Diagram

The J and K inputs shown without connection are for reference only and are functionally at a HIGH level.

Fig8.25: Functional table of 7490

7490 has an inbuilt divide by two and divide by five counters which can be connected in different fashion by changing the connections. It can be used as a divide by 10 counter by connecting Q_A with (clock) input2, grounding all the reset pins, and giving pulse at (clock) input1. This enables the cascade connection of the inbuilt counters. It can also be used as a divide by 6 counter by connecting Q_A with input2, grounding R_3& R_4, and giving pulse at input1.

By connecting Q_A with input1, 7490 can be used for BCD counting whereas by connecting Q_D with input2, it can be used for bi-quinary counting. Bi-quinary is a system for storing decimal digits in a four-bit binary number. The bi-quinary code was used in the abacus. The functional table is shown in fig 8.25.

SYNCHRONOUS COUNTER

In synchronous counter the clock input is connected to all of the flip-flops so that they are clocked simultaneously.

Available synchronous counter ICs are:

IC No.	Description
74160	Decade UP counter
74161	4 bit binary UP counter
74162	Decade UP counter
74163	4 bit binary UP counter
74168, 74192	Decade UP/DOWN counter
74169, 74191, 74193	4 bit binary UP/DOWN counter
74100	Decade UP/DOWN counter

74161 4-bit BINARY COUNTER

The 74161 IC package contains a single 4 bit synchronous counter circuit with a usercontrollable CLR function (pin 1). Unlike the 74163, the clear is asynchronous, or in other words, it takes place immediately, regardless of the status of the clock input. Multiple units can be cascaded to form larger registering synchronous counters.

The pin diagram and internal structure is shown in fig 8.26. This counter IC can be preloaded to start at any value (decimal 0-15, binary 0000-1111). Once load sequence is complete, clock impulses received on the CLK pin will perform a counting operation and will be represented on QA, QB, QC, and QD.

Applications include, digital counters, frequency counters, digital clocks, program counters,

memory addressors, and others where high performance, glitch-free, counting is required.

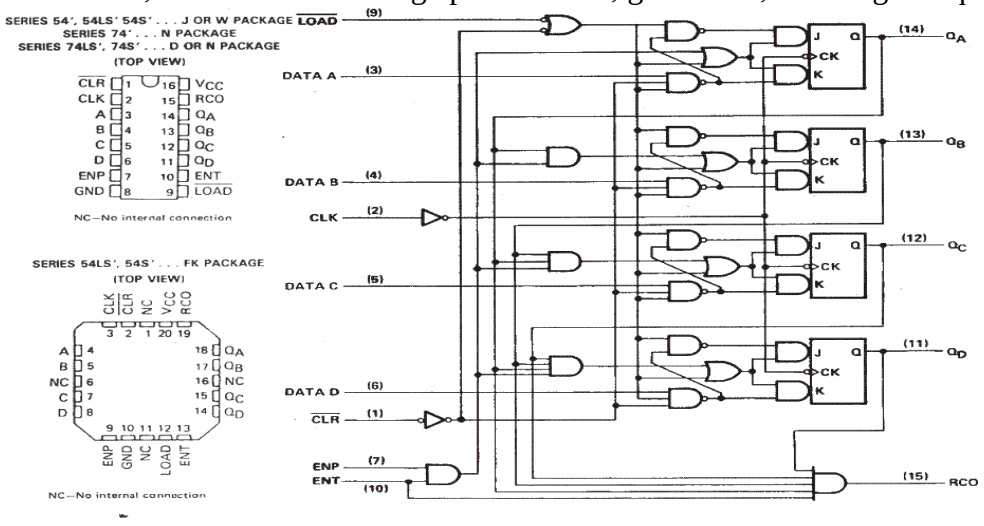


Fig 8.26: 74161 IC pin diagram and internal Structure

74160 DECADE UP COUNTER

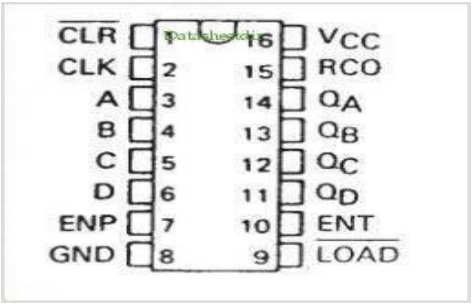


Fig 8.27: pin diagram of
74160

The 74LS160 IC package (fig 8.27), consisting of 16 pins, contains a single 4 bit synchronous counter circuit which can be wired for decade counting mod, without external logic chips. By wiring more than one 74LS160 together (cascading), it is possible to make higher count lengths (powers of ten). For example, two 74LS160s cascaded together would yield a counter capable of decimally counting the range 00-99.This counter IC can be cleared (set to all zero) at any time, by bringing the clear input to logical zero (ground). During normal operation, such as counting mode, the clear input must be kept high either directly or through a pull up resistor.